

The Semantics of x86 Multiprocessor Machine Code

The HOL Specification

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October 30, 2008

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Introduction

This document is an automatically typeset version of the HOL definitions described in the paper:

The Semantics of x86 Multiprocessor Machine Code. Susmit Sarkar, Peter Sewell, Francesco Zappa Nardelli, Scott Owens, Tom Ridge, Thomas Braibant, Magnus Myreen, Jade Alglave. In Proc. POPL 2009.

That paper, and the full HOL definitions, are available from <http://www.cl.cam.ac.uk/users/pes20/weakmemory>. The README from the HOL tarball is reproduced below.

README-spec-public

Here are the HOL sources for the x86 multiprocessor semantics.

To Build
=====

It is known to work with (at least) HOL revision 6031, in the recent PolyML port. To build it, first, install PolyML 5.2 from

http://sourceforge.net/project/showfiles.php?group_id=148318

with something like the following:

```
wget http://downloads.sourceforge.net/polym1/polym1.5.2.tar.gz?modtime=1214245187&big_mirror=0
tar -zxvf polym1.5.2.tar.gz
cd polym1.5.2
./configure --prefix=/usr
make
sudo make install
```

(you may need a different prefix, and/or to ensure that your PATH contains the install directory/bin and your LD_LIBRARY_PATH contains the install directory/lib)

Then install HOL into a directory HOL-poly with something like:

```
svn co https://hol.svn.sf.net/svnroot/hol/HOL HOL-poly
cd HOL-poly
poly < tools-poly/smart-configure.sml
bin/build -expk -symlink
```

(ignore the mllex error at the end), and ensure that HOL-poly/bin is in your PATH. Add `-r6031` after "co" above to get that particular version of HOL.

Finally, just type "make" in this directory (this takes around 15min on an Intel Core2 2.4Ghz machine).

Contents

=====

An automatically typeset version of the definitions

alldoc.ps

alldoc.pdf

This includes the HOL definitions in the files below, except those marked [*]. The HOL proof scripts are not typeset.

The definition of the semantics

x86_coretypesScript.sml

core type definitions, shared by the sequential and event-based semantics

x86_typesScript.sml

types for the event-based semantics: event, event_structure, execution_witness, etc.

x86_astScript.sml

abstract syntax (AST) for x86 instructions

x86_axiomatic_modelScript.sml

the x86-cc axiomatic memory model

x86_niceness_statementScript.sml

the definition of "nice" x86-cc executions

x86_seq_monadScript.sml

the sequential state monad type constructor and combinators

x86_event_monadScript.sml

the event monad type constructor and combinators

x86_opsemScript.sml

the operational semantics for x86 AST instructions, above one of the monads

x86_decoderScript.sml

decoding from machine code bytes to x86 AST assembly instructions

x86_Script.sml

the top level for the sequential semantics

x86_programScript.sml

the top level for the event semantics

The proof that the semantics builds well-formed event structures

x86_event_opsem_wfScript.sml [*]
x86_program_event_structure_wfScript.sml [*]

The proof that the axiomatic model is equivalent to one restricted to nice executions

tactic.sml [*]
x86_niceness_proofScript.sml [*]

The data-race-freedom development

x86_sequential_axiomatic_modelScript.sml
the definition of sequential execution used in the data-race-freedom development

x86_axiomatic_model_thmsScript.sml [*]
auxiliary theorems about the axiomatic model, used in the data-race-freedom development

x86_drfScript.sml
the statements and proof scripts for the main data-race-freedom theorems

An abstract machine that corresponds to the axiomatic memory model

x86_hb_machineScript.sml
the hb machine definition

x86_lts_opsScript.sml
auxiliary definitions for operations over labelled transition systems

x86_hb_machine_thmsScript.sml
statements of theorems about the hb machine, and hand proofs thereof

Other auxiliary files

bit_listScript.sml [*]
decoderScript.sml [*]
opmonScript.sml [*]
utilScript.sml [*]
utilLib.sig [*]

utilLib.sml [*]
HolDoc.sml [*]
HolDoc.sig [*]

README-spec-public
 this file

LICENSE-spec-public
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Part I
x86_coretypes

type_abbrev Ximm : word32

Xreg = EAX | EBX | ECX | EDX | ESP | EBP | ESI | EDI

Xeflags = X_CF | X_PF | X_AF | X_ZF | X_SF | X_OF

Xea =

XEA_I **of** Ximm(* constant *)

| XEA_R **of** Xreg(* register name *)

| XEA_M **of** word32(* memory address *)

type_abbrev proc : num

type_abbrev program_order_index : num

iid = { proc : proc;
 program_order_index : num }

Part II
x86_types

type_abbrev address : Ximm

type_abbrev value : Ximm

type_abbrev eiid : num

type_abbrev reln : 'a#a' → bool

reg = REG32 of Xreg | REG1 of Xeflags | REGEIP

dirn = R | W

location = LOCATION_REG of proc reg
| LOCATION_MEM of address

barrier = LFENCE | SFENCE | MFENCE

action = ACCESS of dirn location value

event = { eiid : eiid;
iid : iid;
action : action }

event_structure = { procs : proc set;
events : event set;
intra_causality : event reln;
atomicity : event set set }

type_abbrev state_constraint : location → value option

type_abbrev view_orders : proc → event reln

execution_witness =
{ initial_state : state_constraint;
vo : view_orders;
write_serialization : event reln;
lock_serialization : event reln;
rfmap : event reln }

type_abbrev eiid_state : eiid set

$$(\text{next_eiid} : \text{eiid_state} \rightarrow (\text{eiid}\#\text{eiid_state})\text{set})\text{eiids} = \{(\text{eiid}, \text{eiids} \cup \{\text{eiid}\}) \mid \text{eiid} \mid \neg(\text{eiid} \in \text{eiids})\}$$

$$(\text{initial_eiid_state} : \text{eiid_state}) = \{\}$$

machine_visible_label =

$$\langle\langle \text{mvl_event} : \text{event};$$

$$\text{mvl_iico} : \text{event set};$$

$$\text{mvl_first_of_instruction} : \text{bool};$$

$$\text{mvl_last_of_instruction} : \text{bool};$$

$$\text{mvl_locked} : \text{bool}\rangle\rangle$$

lts_monad_visible_label =

$$\langle\langle \text{lmvl_iicd} : \text{iicd};$$

$$\text{lmvl_action} : \text{action}\rangle\rangle$$

label = VIS of 'a | TAU

type_abbrev machine_label : machine_visible_label label

type_abbrev lts_monad_label : lts_monad_visible_label label

LTS = $\langle\langle \text{states} : 'state \text{ set};$
 $\text{initial} : 'state;$
 $\text{final} : ('state\# 'value)\text{set};$
 $\text{trans} : ('state\# ('visible \text{ label})\# 'state)\text{set}\rangle\rangle$

Part III
x86_ast

Xrm = XR **of** Xreg(* register *)
 | XM **of** (word2#Xreg) option Xreg option Ximm(* mem[2^{scale} * index + base + displacement] *)

(rm_is_memory_access(XM *i b d*) = **T**) \wedge
 (rm_is_memory_access(XR *r*) = **F**)

Xdest_src = XRM_LI **of** Xrm Ximm(* mnemonic r/m32, imm32 or mnemonic r/m32, imm8 (sign-extended) *)
 | XRM_LR **of** Xrm Xreg(* mnemonic r/m32, r32 *)
 | XR_RM **of** Xreg Xrm(* mnemonic r32, r/m32 *)

Ximm_rm = XLRM **of** Xrm(* r/m32 *)
 | XI **of** Ximm(* imm32 or imm8 (sign-extended) *)

Xbinop_name = XADD | XAND | XCMP | XOR | XSHL | XSHR | XSAR | XSUB | XTEST | XXOR

Xmonop_name = XDEC | XINC | XNOT | XNEG

Xcond = X_ALWAYS | X_E | X_NE

Xinstruction = XBINOP **of** Xbinop_name Xdest_src
 | XMONOP **of** Xmonop_name Xrm
 | XCMPXCHG **of** Xrm Xreg
 | XXADD **of** Xrm Xreg
 | XXCHG **of** Xrm Xreg
 | XLEA **of** Xdest_src
 | XPOP **of** Xrm
 | XPUSH **of** Ximm_rm
 | XCALL **of** Ximm_rm
 | XRET **of** Ximm
 | XMOV **of** Xcond Xdest_src
 | XJUMP **of** Xcond Ximm
 | XLOOP **of** Xcond Ximm(* Here Xcond over approximates possibilities *)
 | XPUSHAD
 | XPOPAD

Xpre_g1 = XLOCK | XG1_NONE

Xpre_g2 = XBRANCH_TAKEN | XBRANCH_NOT_TAKEN | XG2_NONE

Xinst = XPREFIX **of** Xpre_g1 Xpre_g2 Xinstruction

Part IV

x86_axiomatic_model

loc $e =$

case $e.action$ **of**
 ACCESS $d\ l\ v \rightarrow$ SOME l
 || $_ \rightarrow$ NONE

value_of $e =$

case $e.action$ **of**
 ACCESS $d\ l\ v \rightarrow$ SOME v
 || $_ \rightarrow$ NONE

proc $e = e.iid.proc$

mem_load $e =$

case $e.action$ **of**
 ACCESS R(LOCATION_MEM a) $v \rightarrow$ **T**
 || $_ \rightarrow$ **F**

mem_store $e =$

case $e.action$ **of**
 ACCESS W(LOCATION_MEM a) $v \rightarrow$ **T**
 || $_ \rightarrow$ **F**

mem_barrier $e =$

case $e.action$ **of**
 (* Barrier $bar \rightarrow$ **T** || *)
 $_ \rightarrow$ **F**

iiids $E = \{e.iid \mid e \in E.events\}$

writes $E = \{e \mid e \in E.events \wedge \exists l\ v. e.action = \text{ACCESS W } l\ v\}$

reads $E = \{e \mid e \in E.events \wedge \exists l\ v. e.action = \text{ACCESS R } l\ v\}$

locked $E\ e = (e \in \mathbf{bigunion}\ E.atomicity)$

po $E =$

$\{(e_1, e_2) \mid (e_1.iid.proc = e_2.iid.proc) \wedge$
 $e_1.iid.program_order_index \leq e_2.iid.program_order_index \wedge$
 $e_1 \in E.events \wedge e_2 \in E.events\}$

po_strict $E =$

$\{(e_1, e_2) \mid (e_1.iid.proc = e_2.iid.proc) \wedge$
 $e_1.iid.program_order_index < e_2.iid.program_order_index \wedge$
 $e_1 \in E.events \wedge e_2 \in E.events\}$

po_iico $E = \text{po_strict } E \cup E.\text{intra_causality}$

well_formed_event_structure $E =$
 $(\forall \text{iiid. finite}\{\text{eiid} \mid \exists e \in (E.\text{events}).(e.\text{iiid} = \text{iiid}) \wedge (e.\text{eiid} = \text{eiid})\}) \wedge$
 $(\text{finite } E.\text{procs}) \wedge$
 $(\forall e \in (E.\text{events}). \text{proc } e \in E.\text{procs}) \wedge$
 $(\forall e_1 e_2 \in (E.\text{events}). (e_1.\text{eiid} = e_2.\text{eiid}) \wedge (e_1.\text{iiid} = e_2.\text{iiid}) \implies (e_1 = e_2)) \wedge$
 $(\text{DOM } E.\text{intra_causality}) \subseteq E.\text{events} \wedge$
 $(\text{range } E.\text{intra_causality}) \subseteq E.\text{events} \wedge$
 $\text{acyclic}(E.\text{intra_causality}) \wedge$
 $(\forall (e_1, e_2) \in (E.\text{intra_causality}). (e_1.\text{iiid} = e_2.\text{iiid})) \wedge$
 $(\forall (e_1, e_2) \in (E.\text{intra_causality}). \neg(\text{mem_store } e_1)) \wedge$
 $(\forall (e_1 \in \text{writes } E) e_2.$
 $\neg(e_1 = e_2) \wedge$
 $(e_2 \in \text{writes } E \vee e_2 \in \text{reads } E) \wedge$
 $(e_1.\text{iiid} = e_2.\text{iiid}) \wedge$
 $(\text{loc } e_1 = \text{loc } e_2) \wedge$
 $(\exists p r. \text{loc } e_1 = \text{SOME } (\text{LOCATION_REG } p r))$
 \implies
 $(e_1, e_2) \in E.\text{intra_causality}^+ \vee$
 $(e_2, e_1) \in E.\text{intra_causality}^+) \wedge$
 $(\forall es \in (E.\text{atomicity}). \exists e \in es. \text{mem_load } e) \wedge$
 $\text{PER } E.\text{events } E.\text{atomicity} \wedge$
 $(\forall es \in (E.\text{atomicity}). \forall e_1 e_2 \in es. (e_1.\text{iiid} = e_2.\text{iiid})) \wedge$
 $(\forall es \in (E.\text{atomicity}). \forall e_1 \in es. \forall e_2 \in (E.\text{events}). (e_1.\text{iiid} = e_2.\text{iiid}) \implies e_2 \in es) \wedge$
 $(\forall e \in (E.\text{events}). \forall p r. (\text{loc } e = \text{SOME } (\text{LOCATION_REG } p r)) \implies (p = \text{proc } e))$

sub_event_structure $E' E =$
 $(E'.\text{procs} = E.\text{procs}) \wedge$
 $E'.\text{events} \subseteq E.\text{events} \wedge$
 $(E'.\text{atomicity} = \text{PER_RESTRICT } E.\text{atomicity } E'.\text{events}) \wedge$
 $(E'.\text{intra_causality} = E.\text{intra_causality}|_{E'.\text{events}})$

preserved_program_order $E =$
 $\{(e_1, e_2) \mid (e_1, e_2) \in (\text{po_strict } E) \wedge$
 $((\exists p r. (\text{loc } e_1 = \text{loc } e_2) \wedge$
 $(\text{loc } e_1 = \text{SOME } (\text{LOCATION_REG } p r)))) \vee$
 $(\text{mem_load } e_1 \wedge \text{mem_load } e_2) \vee$
 $(\text{mem_store } e_1 \wedge \text{mem_store } e_2) \vee$
 $(\text{mem_load } e_1 \wedge \text{mem_store } e_2) \vee$
 $(\text{mem_store } e_1 \wedge \text{mem_load } e_2 \wedge (\text{loc } e_1 = \text{loc } e_2)) \vee$
 $((\text{mem_load } e_1 \vee \text{mem_store } e_1) \wedge \text{locked } E e_2) \vee$
 $(\text{locked } E e_1 \wedge (\text{mem_load } e_2 \vee \text{mem_store } e_2))\}\}$

viewed_events $E p =$
 $\{e \mid e \in E.\text{events} \wedge ((\text{proc } e = p) \vee \text{mem_store } e)\}$

view_orders_well_formed E $vo =$
 $(\forall p \in (E.procs). \text{linear_order}(vo\ p)(\text{viewed_events } E\ p) \wedge$
 $\quad \forall e \in (\text{viewed_events } E\ p). \mathbf{finite}\{e' \mid (e', e) \in (vo\ p)\}) \wedge$
 $(\forall p. \neg(p \in E.procs) \implies (vo\ p = \{\}))$

get_l_stores E $l =$
 $\{e \mid e \in E.events \wedge \text{mem_store } e \wedge (\text{loc } e = \text{SOME } l)\}$

write_serialization_candidates_old $E =$
let $per_location_store_sets = \{es \mid \exists l. es = \text{get_l_stores } E\ l\}$ **in**
let $per_location_store_set_linearisations = \{\text{strict_linearisations } es \mid es \in per_location_store_sets\}$ **in**
let $choices = all_choices\ per_location_store_set_linearisations$ **in**
 $\{\mathbf{bigunion } lin \mid lin \in choices\}$

write_serialization_candidates E $cand =$
 $(\forall (e_1, e_2) \in cand.$
 $\quad \exists l. e_1 \in (\text{get_l_stores } E\ l) \wedge e_2 \in (\text{get_l_stores } E\ l) \wedge$
 $(\forall l. \text{strict_linear_order}(cand|_{(\text{get_l_stores } E\ l)})$
 $\quad (\text{get_l_stores } E\ l))$

lock_serialization_candidates $E =$
let $lin_ec = \text{strict_linearisations } E.atomicity$ **in**
 $\{\{(e_1, e_2) \mid \exists (es_1, es_2) \in lin. e_1 \in es_1 \wedge e_2 \in es_2\}$
 $\quad \mid lin \in lin_ec\}$

reads_from_map_candidates_old $E =$
let $reads_and_their_possible_writes =$
 $\{(er, ews) \mid er \in E.events \wedge$
 $\quad \exists l v. (er.action = \text{ACCESS R } l\ v) \wedge$
 $\quad (ews = \{ew \mid ew \in E.events \wedge (ew.action = \text{ACCESS W } l\ v)\})\}$ **in**
 $\{rfmap \mid (\mathbf{range } rfmap) \subseteq (DOM\ reads_and_their_possible_writes) \wedge$
 $\quad \forall (ew, er) \in rfmap. \exists ews. (er, ews) \in reads_and_their_possible_writes \wedge ew \in ews\}$

reads_from_map_candidates E $rfmap =$
 $\forall (ew, er) \in rfmap. er \in E.events \wedge ew \in E.events \wedge$
 $\quad \exists l v. (er.action = \text{ACCESS R } l\ v) \wedge$
 $\quad (ew.action = \text{ACCESS W } l\ v)$

happens_before E $X =$
 $E.intra_causality \cup$
 $(\text{preserved_program_order } E) \cup$
 $X.write_serialization \cup$
 $X.lock_serialization \cup$
 $X.rfmap$

check_causality E *vo happensbefore* =
 $\forall p \in (E.procs). \text{acyclic}((\text{strict}(vo\ p)) \cup \text{happensbefore})$

check_rfmap_written E *vo rfmap* =
 $\forall p \in (E.procs).$
 $\forall (ew, er) \in (rfmap|_{(\text{viewed_events } E\ p)}).$
 $\forall ew' \in (\text{writes } E).$
 $\neg(ew = ew') \wedge (ew, ew') \in (vo\ p) \wedge (ew', er) \in (vo\ p)$
 $\implies \neg(\text{loc } ew = \text{loc } ew')$

check_rfmap_initial E *vo rfmap initial_state* =
 $\forall p \in (E.procs).$
 $\forall er \in ((\text{reads } E) \setminus (\text{range } rfmap))$
 $\cap \text{viewed_events } E\ p).$
 $\exists l\ v.(er.action = \text{ACCESS } R\ l\ v) \wedge$
 $(\text{initial_state } l = \text{SOME } v) \wedge$
 $\forall ew' \in \text{writes } E.$
 $(ew', er) \in (vo\ p) \implies \neg(\text{loc } ew' = \text{loc } er)$

state_updates E *vo write_serialization l* =
case l **of**
 LOCATION_MEM $a \rightarrow$
 $\{\text{value_of } ew \mid ew \in \text{maximal_elements}(\text{get_l_stores } E\ l)\text{write_serialization}\}$
 || LOCATION_REG $p\ r \rightarrow$
 $\{\text{value_of } ew \mid ew \in \text{maximal_elements}(\text{get_l_stores } E\ l)(vo\ p)\}$

check_final E *vo initial_state final_state_opt write_serialization* =
if **finite** $E.events$ **then**
 $\exists \text{final_state} . (\text{final_state_opt} = \text{SOME } \text{final_state}) \wedge$
 $\forall l. \text{if } (\text{state_updates } E\ \text{vo } \text{write_serialization } l) = \{\}$ **then**
 $\text{final_state } l = \text{initial_state } l$
else
 $(\text{final_state } l) \in (\text{state_updates } E\ \text{vo } \text{write_serialization } l)$
else
 $\text{final_state_opt} = \text{NONE}$

state_updates_mem E *write_serialization a* =
 $\{\text{value_of } ew \mid ew \in \text{maximal_elements}(\text{get_l_stores } E(\text{LOCATION_MEM } a))\text{write_serialization}\}$

$(\text{check_final_mem } E\ \text{initial_state } \text{write_serialization } \text{NONE} =$
 $\neg(\text{finite } E.events)) \wedge$
 $(\text{check_final_mem } E\ \text{initial_state } \text{write_serialization}(\text{SOME } \text{final_state}) =$
finite $E.events \wedge$
 $\forall a. \text{if } (\text{state_updates_mem } E\ \text{write_serialization } a) = \{\}$ **then**
 $\text{final_state } a = \text{initial_state}(\text{LOCATION_MEM } a)$
else
 $(\text{final_state } a) \in (\text{state_updates_mem } E\ \text{write_serialization } a))$

check_atomicity E vo =
 $\forall p \in (E.procs). \forall es \in (E.atomicity).$
 $\forall e_1 e_2 \in es. (e_1, e_2) \in (vo p) \implies$
 $\forall e. (e_1, e) \in (vo p) \wedge (e, e_2) \in (vo p) \implies e \in es$

valid_execution E X =
view_orders_well_formed E $X.vo$ \wedge
 $X.write_serialization \in write_serialization_candidates E \wedge$
 $X.lock_serialization \in lock_serialization_candidates E \wedge$
 $X.rfmap \in reads_from_map_candidates E \wedge$
check_causality E $X.vo$ (happens_before E X) \wedge
check_rfmap_written E $X.vo$ $X.rfmap$ \wedge
check_rfmap_initial E $X.vo$ $X.rfmap$ $X.initial_state$ \wedge
check_atomicity E $X.vo$

restrict_execution_witness X E =
 $\llbracket initial_state := X.initial_state;$
 $(*final_state_opt := ... *)$
 $vo := (\lambda p. (X.vo p)|_{E.events});$
 $write_serialization := X.write_serialization|_{E.events};$
 $lock_serialization := X.lock_serialization|_{E.events};$
 $rfmap := RRESTRICT X.rfmap E.events \rrbracket$

Part V

x86_niceness_statement

nice_execution $E X = \forall p \in (E.procs).$
 $(po_strict E)|_{(viewed_events E p \setminus mem_store)} \subseteq (X.vo p)$

niceness_thm =
 $\forall E X. (well_formed_event_structure E \wedge$
 $valid_execution E X) \implies$
 $\exists X'. valid_execution E X' \wedge nice_execution E X' \wedge$
 $(X' \llbracket vo := (\lambda p. \{\}) \rrbracket = X \llbracket vo := (\lambda p. \{\}) \rrbracket)$

Part VI

x86_seq_monad

type_abbrev x86_state : (Xreg → word32)#(* - general-purpose 32-bit registers *)
(word32)#(* - eip *)
(Xeflags → bool option)#(* - eflags *)
(word32 → word8 option)(* - unsegmented memory *)

XREAD_REG $i((r, eip, f, m) : \text{x86_state}) = r \ i$

XREAD_EIP $((r, eip, f, m) : \text{x86_state}) = eip$

XREAD_EFLAG $i((r, eip, f, m) : \text{x86_state}) = f \ i$

XREAD_MEM $i((r, eip, f, m) : \text{x86_state}) = m \ i$

XWRITE_REG $i \ x((r, eip, f, m) : \text{x86_state}) = ((i = +x)r, eip, f, m) : \text{x86_state}$

XWRITE_EIP $x((r, eip, f, m) : \text{x86_state}) = (r, x, f, m) : \text{x86_state}$

XWRITE_EFLAG $i \ x((r, eip, f, m) : \text{x86_state}) = (r, eip, (i = +x)f, m) : \text{x86_state}$

XWRITE_MEM $i \ x((r, eip, f, m) : \text{x86_state}) = (r, eip, f, (i = +x)m) : \text{x86_state}$

XREAD_MEMBYTES $n \ a \ s =$

if $n = 0$ **then** [] **else** XREAD_MEM $a \ s \in$ XREAD_MEM_BYTES $(n - 1)(a + 1w)s$

type_abbrev M : x86_state → ('a#x86_state) option

(constT_seq : 'a → 'a M) $x = \lambda y.$ SOME (x, y)

(addT_seq : 'a → 'b M → ('a#'b)M) $x \ s =$
 $\lambda y.$ **case** $s \ y$ **of** NONE → NONE || SOME $(z, t) \rightarrow$ SOME $((x, z), t)$

(lockT_seq : 'a M → 'a M) $s = s$

(failureT_seq : 'a M) = $\lambda y.$ NONE

(seqT_seq : 'a M → ('a → 'b M) → 'b M) $s \ f =$
 $\lambda y.$ **case** $s \ y$ **of** NONE → NONE || SOME $(z, t) \rightarrow$ $f \ z \ t$

(parT_seq : 'a M → 'b M → ('a#'b)M) $s \ t =$
 $\lambda y.$ **case** $s \ y$ **of** NONE → NONE || SOME $(a, z) \rightarrow$
case $t \ z$ **of** NONE → NONE || SOME $(b, x) \rightarrow$ SOME $((a, b), x)$


```
(parT_unit_seq : unit M → unit M → unit M)s t =
λy.case s y of NONE → NONE || SOME (a, z) →
  case t z of NONE → NONE || SOME (b, x) → SOME ((), x)
```

```
(write_reg_seq ii r x) : unit M =
λs.SOME ((), XWRITE_REG r x s)
```

```
(read_reg_seq ii r) : Ximm M =
λs.SOME (XREAD_REG r s, s)
```

```
(write_eflag_seq ii f x) : unit M =
(λs.SOME ((), XWRITE_EFLAG f x s))
```

```
(read_eflag_seq ii f) : bool M =
(λs.case XREAD_EFLAG f s of NONE → NONE || SOME b → SOME (b, s))
```

```
(write_eip_seq ii x) : unit M =
λs.SOME ((), XWRITE_EIP x s)
```

```
(read_eip_seq ii) : Ximm M =
λs.SOME (XREAD_EIP s, s)
```

```
(write_mem_seq ii a x) : unit M =
(λs.case XREAD_MEM a s of NONE → NONE || SOME y → SOME ((), XWRITE_MEM a (SOME x)s))
```

```
(read_mem_seq ii a) : word8 M =
(λs.case XREAD_MEM a s of NONE → NONE || SOME x → SOME (x, s))
```

```
(read_m32_seq ii a) : Ximm M =
seqT_seq(parT_seq(read_mem_seq ii(a + 0w))(parT_seq(read_mem_seq ii(a + 1w))
  (parT_seq(read_mem_seq ii(a + 2w))(read_mem_seq ii(a + 3w))))))
  (λ(x0, x1, x2, x3). constT_seq(bytes2word[x0; x1; x2; x3]))
```

```
(write_m32_seq ii a w) : unit M =
(let bs = word2bytes 4 w in
  parT_unit_seq(write_mem_seq ii(a + 0w)(EL 0 bs))(parT_unit_seq(write_mem_seq ii(a + 1w)(EL 1 bs))
  (parT_unit_seq(write_mem_seq ii(a + 2w)(EL 2 bs))(write_mem_seq ii(a + 3w)(EL 3 bs))))))
```

```
(constT : 'a → 'a M) = constT_seq
```

```
(addT : 'a → 'b M → ('a#'#b)M) = addT_seq
```

(lockT : unit M → unit M) = lockT_seq

(failureT : unit M) = failureT_seq

(seqT : 'a M → ('a → 'b M) → 'b M) = seqT_seq

(parT : 'a M → 'b M → ('a#b)M) = parT_seq

(parT_unit : unit M → unit M → unit M) = parT_unit_seq

(write_reg : iid → Xreg → Ximm → unit M) = write_reg_seq

(read_reg : iid → Xreg → Ximm M) = read_reg_seq

(write_eip : iid → Ximm → unit M) = write_eip_seq

(read_eip : iid → Ximm M) = read_eip_seq

(write_eflag : iid → Xeflags → bool option → unit M) = write_eflag_seq

(read_eflag : iid → Xeflags → bool M) = read_eflag_seq

(write_m32 : iid → Ximm → Ximm → unit M) = write_m32_seq

(read_m32 : iid → Ximm → Ximm M) = read_m32_seq

option_apply x f = **if** x = NONE **then** NONE **else** f(**the** x)

Part VII

x86_event_monad

type_abbrev M : iid_state \rightarrow ((iid_state#'a#event_structure)set)

event_structure_empty = $\langle\langle$ procs := {}; events := {}; intra_causality := {}; atomicity := {} $\rangle\rangle$

event_structure_lock es = $\langle\langle$ procs := es.procs; events := es.events; intra_causality := es.intra_causality; atomicity := if

event_structure_union es₁ es₂ =
 $\langle\langle$ procs := es₁.procs \cup es₂.procs;
 events := es₁.events \cup es₂.events;
 intra_causality := es₁.intra_causality \cup es₂.intra_causality;
 atomicity := es₁.atomicity \cup es₂.atomicity $\rangle\rangle$

event_structure_bigunion(ess : event_structure set) =
 $\langle\langle$ procs := **bigunion**{es.procs | es \in ess};
 events := **bigunion**{es.events | es \in ess};
 intra_causality := **bigunion**{es.intra_causality | es \in ess};
 atomicity := **bigunion**{es.atomicity | es \in ess} $\rangle\rangle$

event_structure_seq_union es₁ es₂ =
 $\langle\langle$ procs := es₁.procs \cup es₂.procs;
 events := es₁.events \cup es₂.events;
 intra_causality := es₁.intra_causality
 \cup es₂.intra_causality
 \cup {(e₁, e₂)
 | e₁ \in (maximal_elements es₁.events es₁.intra_causality)
 \wedge e₂ \in (minimal_elements es₂.events es₂.intra_causality)} $\rangle\rangle$;
 atomicity := es₁.atomicity \cup es₂.atomicity

(mapT_ev : ('a \rightarrow 'b) \rightarrow 'a M \rightarrow 'b M)f s =

λ iid_next : iid_state.

let t = s iid_next **in**
 {(iid_next', f x, es)
 | (iid_next', x, es) \in t}

(choiceT_ev : 'a M \rightarrow 'a M \rightarrow 'a M)s s' =

λ iid_next : iid_state.s iid_next \cup s' iid_next

(constT_ev : 'a \rightarrow 'a M)x = λ iid_next.{(iid_next, x, event_structure_empty)}

(discardT_ev : 'a M \rightarrow unit M)s =

λ iid_next.**let** (t : (iid_state#'a#event_structure)set) = s iid_next **in**
image(λ (iid_next', v, es).(iid_next', (), es))t

(addT_ev : 'a → 'b M → ('a#'b)M)x s =
 $\lambda e_{iid_next}.$ let (t : (e_{iid_state}#'b#event_structure)set) = s e_{iid_next} in
 image($\lambda(e_{iid_next}', v, es).$ (e_{iid_next}', (x, v), es))t

(lockT_ev : 'a M → 'a M)s =
 $\lambda e_{iid_next}.$ let (t : (e_{iid_state}#'a#event_structure)set) = s e_{iid_next} in
 image($\lambda(e_{iid_next}', v, es).$ (e_{iid_next}', v, event_structure_lock es))t

(failureT_ev : 'a M) = $\lambda e_{iid_next}.$ {}

(seqT_ev : 'a M → ('a → 'b M) → 'b M)s f =
 $\lambda e_{iid_next} :$ e_{iid_state}.

let t = s e_{iid_next} in
 bigunion{let t' = f x e_{iid_next}' in
 {(e_{iid_next}'', x', event_structure_seq_union es es')
 | (e_{iid_next}'', x', es') ∈ t'}
 | (e_{iid_next}', x, es) ∈ t}

(parT_ev : 'a M → 'b M → ('a#'b)M)s s' =
 $\lambda e_{iid_next} :$ e_{iid_state}.

let t = s e_{iid_next} in
 bigunion{let t' = s' e_{iid_next}' in
 {(e_{iid_next}'', (x, x'), event_structure_union es es')
 | (e_{iid_next}'', x', es') ∈ t'}
 | (e_{iid_next}', x, es) ∈ t}

(parT_unit_ev : unit M → unit M → unit M)s s' =
 $\lambda e_{iid_next} :$ e_{iid_state}.

let t = s e_{iid_next} in
 bigunion{let t' = s' e_{iid_next}' in
 {(e_{iid_next}'', (), event_structure_union es es')
 | (e_{iid_next}'', (), es') ∈ t'}
 | (e_{iid_next}', (), es) ∈ t}

(write_location_ev ii l x) : unit M =

$\lambda e_{iid_next}.$ {(e_{iid_next}',
 (),
 {procs := {ii.proc};
 events := { {e_{iid} := e_{iid}';
 i_{iid} := ii;
 action := ACCESS W l x} };
 intra_causality := {};
 atomicity := {} } | (e_{iid}', e_{iid_next}') ∈ next_e_{iid} e_{iid_next}}

```

(read_location_ev ii l) : value M =
λeiiid_next.{(eiiid_next',
  x,
  ⟨⟦ procs := {ii.proc};
  events := {⟦ eiiid := eiiid';
              iiid := ii;
              action := ACCESS R l x ⟧};
  intra_causality := {};
  atomicity := {} ⟧⟩)
| x ∈ UNIV ∧ (eiiid', eiiid_next') ∈ next_eiid eiiid_next}

```

```

(write_reg_ev ii r x) : unit M =
write_location_ev ii (LOCATION_REG ii.proc (REG32 r)) x

```

```

(read_reg_ev ii r) : value M =
read_location_ev ii (LOCATION_REG ii.proc (REG32 r))

```

```

(write_eip_ev ii x) : unit M =
write_location_ev ii (LOCATION_REG ii.proc REGEIP) x

```

```

(read_eip_ev ii) : value M =
read_location_ev ii (LOCATION_REG ii.proc REGEIP)

```

```

(write_eflag_ev ii f bo) : unit M =
case bo of
SOME b →
(write_location_ev ii (LOCATION_REG ii.proc (REG1 f)) (if b then 1w else 0w))
|| NONE →
choiceT_ev
  (write_location_ev ii (LOCATION_REG ii.proc (REG1 f)) 0w)
  (write_location_ev ii (LOCATION_REG ii.proc (REG1 f)) 1w)

```

```

(read_eflag_ev ii f) : bool M =
mapT_ev (λx.(x = 0w))
(read_location_ev ii (LOCATION_REG ii.proc (REG1 f)))

```

```

aligned32 a = ((a && 3w) = 0w)

```

```

(write_m32_ev ii a x) : unit M =
if aligned32 a then
write_location_ev ii (LOCATION_MEM a) x
else
failureT_ev

```

```

(read_m32_ev ii a) : Ximm M =
if aligned32 a then
  read_location_ev ii (LOCATION_MEM a)
else
  failureT_ev

```

```

(constT : 'a → 'a M) = constT_ev

```

```

(addT : 'a → 'b M → ('a##'b)M) = addT_ev

```

```

(lockT : unit M → unit M) = lockT_ev

```

```

(failureT : unit M) = failureT_ev

```

```

(seqT : 'a M → (('a → 'b M) → 'b M)) = seqT_ev

```

```

(parT : 'a M → 'b M → ('a##'b)M) = parT_ev

```

```

(parT_unit : unit M → unit M → unit M) = parT_unit_ev

```

```

(write_reg : iid → Xreg → Ximm → unit M) = write_reg_ev

```

```

(read_reg : iid → Xreg → Ximm M) = read_reg_ev

```

```

(write_eip : iid → Ximm → unit M) = write_eip_ev

```

```

(read_eip : iid → Ximm M) = read_eip_ev

```

```

(write_eflag : iid → Xeflags → bool option → unit M) = write_eflag_ev

```

```

(read_eflag : iid → Xeflags → bool M) = read_eflag_ev

```

```

(write_m32 : iid → Ximm → Ximm → unit M) = write_m32_ev

```

```

(read_m32 : iid → Ximm → Ximm M) = read_m32_ev

```

Part VIII
x86_opsem

$$\text{ea_Xr}(r : \text{Xreg}) = \text{constT}(\text{XEA_R } r)$$

$$\text{ea_Xi}(i : \text{Ximm}) = \text{constT}(\text{XEA_I } i)$$

$$\begin{aligned} &(\text{ea_Xrm_base } ii \text{ NONE} = \text{constT } 0w) \wedge \\ &(\text{ea_Xrm_base } ii(\text{SOME } r) = \text{read_reg } ii \ r) \end{aligned}$$

$$\begin{aligned} &(\text{ea_Xrm_index } ii \text{ NONE} = \text{constT}(0w : \text{Ximm})) \wedge \\ &(\text{ea_Xrm_index } ii(\text{SOME } (s : \text{word2}, r)) = \\ &\text{seqT}(\text{read_reg } ii \ r)(\lambda idx. \text{constT}(\mathbf{n2w}(2 ** \mathbf{w2n } s) * idx))) \end{aligned}$$

$$\begin{aligned} &(\text{ea_Xrm } ii(\text{XR } r) = \text{ea_Xr } r) \wedge \\ &(\text{ea_Xrm } ii(\text{XM } i \ b \ d) = \\ &\text{seqT} \\ &\quad (\text{parT}(\text{ea_Xrm_index } ii \ i)(\text{ea_Xrm_base } ii \ b)) \\ &\quad (\lambda(idx, b). \text{constT}(\text{XEA_M}(idx + b + d)))) \end{aligned}$$

$$\begin{aligned} &(\text{ea_Xdest } ii(\text{XRM_I } rm \ i) = \text{ea_Xrm } ii \ rm) \wedge \\ &(\text{ea_Xdest } ii(\text{XRM_R } rm \ r) = \text{ea_Xrm } ii \ rm) \wedge \\ &(\text{ea_Xdest } ii(\text{XR_RM } r \ rm) = \text{ea_Xr } r) \end{aligned}$$

$$\begin{aligned} &(\text{ea_Xsrc } ii(\text{XRM_I } rm \ i) = \text{ea_Xi } i) \wedge \\ &(\text{ea_Xsrc } ii(\text{XRM_R } rm \ r) = \text{ea_Xr } r) \wedge \\ &(\text{ea_Xsrc } ii(\text{XR_RM } r \ rm) = \text{ea_Xrm } ii \ rm) \end{aligned}$$

$$\begin{aligned} &(\text{ea_Ximm_rm } ii(\text{XLRM } rm) = \text{ea_Xrm } ii \ rm) \wedge \\ &(\text{ea_Ximm_rm } ii(\text{XI } i) = \text{ea_Xi } i) \end{aligned}$$

$$\begin{aligned} &(\text{read_ea } ii(\text{XEA_I } i) = \text{constT } i) \wedge \\ &(\text{read_ea } ii(\text{XEA_R } r) = \text{read_reg } ii \ r) \wedge \\ &(\text{read_ea } ii(\text{XEA_M } a) = \text{read_m32 } ii \ a) \end{aligned}$$

$$\text{read_src_ea } ii \ ds = \text{seqT}(\text{ea_Xsrc } ii \ ds)(\lambda ea. \text{addT } ea(\text{read_ea } ii \ ea))$$

$$\text{read_dest_ea } ii \ ds = \text{seqT}(\text{ea_Xdest } ii \ ds)(\lambda ea. \text{addT } ea(\text{read_ea } ii \ ea))$$

$$\begin{aligned} &(\text{write_ea } ii(\text{XEA_I } i)x = \text{failureT}) \wedge (* \text{ one cannot store into a constant } *) \\ &(\text{write_ea } ii(\text{XEA_R } r)x = \text{write_reg } ii \ r \ x) \wedge \\ &(\text{write_ea } ii(\text{XEA_M } a)x = \text{write_m32 } ii \ a \ x) \end{aligned}$$

$$\begin{aligned} &(\text{jump_to_ea } ii \ eip(\text{XEA_I } i) = \text{write_eip } ii(eip + i)) \wedge \\ &(\text{jump_to_ea } ii \ eip(\text{XEA_R } r) = \text{seqT}(\text{read_reg } ii \ r)(\text{write_eip } ii)) \wedge \\ &(\text{jump_to_ea } ii \ eip(\text{XEA_M } a) = \text{seqT}(\text{read_m32 } ii \ a)(\text{write_eip } ii)) \end{aligned}$$

```
(call_dest_from_ea ii eip(XEA_I i) = constT(eip + i)) ∧
(call_dest_from_ea ii eip(XEA_R r) = read_reg ii r) ∧
(call_dest_from_ea ii eip(XEA_M a) = read_m32 ii a)
```

```
(get_ea_address(XEA_I i) = 0w) ∧
(get_ea_address(XEA_R r) = 0w) ∧
(get_ea_address(XEA_M a) = a)
```

```
bump_eip ii len rest =
parT_unit rest(seqT(read_eip ii)(λx. write_eip ii(x + len)))
```

```
byte_parity = EVEN o length o filter I o n2bits 8 o w2n
```

```
write_PF ii w = write_eflag ii X_PF(SOME (byte_parity w))
```

```
write_ZF ii w = write_eflag ii X_ZF(SOME (w = 0w))
```

```
write_SF ii w = write_eflag ii X_SF(SOME (word_msb w))
```

```
write_logical_eflags ii w =
parT_unit(write_PF ii w)
(parT_unit(write_ZF ii w)
(parT_unit(write_SF ii w)
(parT_unit(write_eflag ii X_OF(SOME F))
(parT_unit(write_eflag ii X_CF(SOME F))
(write_eflag ii X_AF NONE))))))
```

```
write_arith_eflags_except_CF ii w =
parT_unit(write_PF ii w)
(parT_unit(write_ZF ii w)
(parT_unit(write_SF ii w)
(parT_unit(write_eflag ii X_OF NONE)
(write_eflag ii X_AF NONE))))
```

```
write_arith_eflags ii(w, c) =
parT_unit(write_eflag ii X_CF(SOME c))(write_arith_eflags_except_CF ii w)
```

```
erase_eflags ii =
parT_unit(write_eflag ii X_PF NONE)
(parT_unit(write_eflag ii X_ZF NONE)
(parT_unit(write_eflag ii X_SF NONE)
(parT_unit(write_eflag ii X_OF NONE)
(parT_unit(write_eflag ii X_CF NONE)
(write_eflag ii X_AF NONE))))))
```

add_with_carry_out($x : \text{Ximm}$) $y = (x + y, 2 * *32 \leq \mathbf{w2n} \ x + \mathbf{w2n} \ y)$

sub_with_borrow_out($x : \text{Ximm}$) $y = (x - y, x < +y)$

write_arith_result $ii(w, c)ea = \text{parT_unit}(\text{write_arith_eflags } ii(w, c))(\text{write_ea } ii \ ea \ w)$

write_arith_result_no_CF $ii \ w \ ea =$
 $(\text{parT_unit}(\text{write_arith_eflags_except_CF } ii \ w))(\text{write_ea } ii \ ea \ w)$

write_arith_result_no_write $ii(w, c) = (\text{write_arith_eflags } ii(w, c))$

write_logical_result $ii \ w \ ea = (\text{parT_unit}(\text{write_logical_eflags } ii \ w))(\text{write_ea } ii \ ea \ w)$

write_logical_result_no_write $ii \ w = (\text{write_logical_eflags } ii \ w)$

write_result_erase_eflags $ii \ w \ ea = (\text{parT_unit}(\text{erase_eflags } ii))(\text{write_ea } ii \ ea \ w)$

$(\text{write_binop } ii \ \text{XADD } x \ y \ ea = (\text{write_arith_result } ii(\text{add_with_carry_out } x \ y)ea)) \wedge$
 $(\text{write_binop } ii \ \text{XSUB } x \ y \ ea = (\text{write_arith_result } ii(\text{sub_with_borrow_out } x \ y)ea)) \wedge$
 $(\text{write_binop } ii \ \text{XCMP } x \ y \ ea = (\text{write_arith_result_no_write } ii(\text{sub_with_borrow_out } x \ y))) \wedge$
 $(\text{write_binop } ii \ \text{XTEST } x \ y \ ea = (\text{write_logical_result_no_write } ii(x \ \& \ y))) \wedge$
 $(\text{write_binop } ii \ \text{XAND } x \ y \ ea = (\text{write_logical_result } ii(x \ \& \ y)ea)) \wedge$
 $(\text{write_binop } ii \ \text{XXOR } x \ y \ ea = (\text{write_logical_result } ii(x \ ?? \ y)ea)) \wedge$
 $(\text{write_binop } ii \ \text{XOR } x \ y \ ea = (\text{write_logical_result } ii(x \ ! \ y)ea)) \wedge$
 $(\text{write_binop } ii \ \text{XSHL } x \ y \ ea = (\text{write_result_erase_eflags } ii(x \ \ll \ \mathbf{w2n} \ y)ea)) \wedge$
 $(\text{write_binop } ii \ \text{XSHR } x \ y \ ea = (\text{write_result_erase_eflags } ii(x \ \gg \ \mathbf{w2n} \ y)ea)) \wedge$
 $(\text{write_binop } ii \ \text{XSAR } x \ y \ ea = (\text{write_result_erase_eflags } ii(x \ \gg \ \mathbf{w2n} \ y)ea))$

$(\text{write_monop } ii \ \text{XNOT } x \ ea = \text{write_ea } ii \ ea(\neg x)) \wedge$
 $(\text{write_monop } ii \ \text{XDEC } x \ ea = \text{write_arith_result_no_CF } ii(x - 1w)ea) \wedge$
 $(\text{write_monop } ii \ \text{XINC } x \ ea = \text{write_arith_result_no_CF } ii(x + 1w)ea) \wedge$
 $(\text{write_monop } ii \ \text{XNEG } x \ ea =$
 $\text{parT_unit}(\text{write_arith_result_no_CF } ii(0w - x)ea)$
 $(\text{write_eflag } ii \ \text{X_CF NONE}))$

$(\text{read_cond } ii \ \text{X_ALWAYS} = \text{constT } \mathbf{T}) \wedge$
 $(\text{read_cond } ii \ \text{X_E} = \text{read_eflag } ii \ \text{X_ZF}) \wedge$
 $(\text{read_cond } ii \ \text{X_NE} = \text{seqT}(\text{read_eflag } ii \ \text{X_ZF})(\lambda b. \text{constT}(\neg b)))$

x86_exec_pop $ii \ rm =$
 $\text{seqT}(\text{seqT}(\text{read_reg } ii \ \text{ESP})(\lambda esp. \text{addT } esp(\text{write_reg } ii \ \text{ESP}(esp + 4w))))$
 $(\lambda(old_esp, x). \text{seqT}(\text{parT}(ea_Xrm } ii \ rm)(\text{read_m32 } ii \ old_esp))$
 $(\lambda(ea, w). \text{write_ea } ii \ ea \ w))$

x86_exec_push *ii imm_rm* =

```
(seqT
  (parT(seqT(ea_Ximm_rm ii imm_rm)( $\lambda ea.$  read_ea ii ea))
    (seqT(read_reg ii ESP)( $\lambda w.$  constT( $w - 4w$ ))))
  ( $\lambda(w, esp).$  parT_unit(write_m32 ii esp w)(write_reg ii ESP esp)))
```

x86_exec_popad *ii* =

```
seqT(read_reg ii ESP)( $\lambda original\_esp.$ 
  parT_unit(write_reg ii ESP( $original\_esp + 32w$ ))(
  parT_unit(seqT(read_m32 ii( $original\_esp$ ))( $\lambda x.$  write_reg ii EDI x))(
  parT_unit(seqT(read_m32 ii( $original\_esp + 4w$ ))( $\lambda x.$  write_reg ii ESI x))(
  parT_unit(seqT(read_m32 ii( $original\_esp + 8w$ ))( $\lambda x.$  write_reg ii EBP x))(
  (* The next 4 bytes of stack (containing saved value of ESP) are skipped*)
  parT_unit(seqT(read_m32 ii( $original\_esp + 16w$ ))( $\lambda x.$  write_reg ii EBX x))(
  parT_unit(seqT(read_m32 ii( $original\_esp + 20w$ ))( $\lambda x.$  write_reg ii EDX x))(
  parT_unit(seqT(read_m32 ii( $original\_esp + 24w$ ))( $\lambda x.$  write_reg ii ECX x))(
    (seqT(read_m32 ii( $original\_esp + 28w$ ))( $\lambda x.$  write_reg ii EAX x)))))))))
```

x86_exec_pushad *ii* =

```
seqT(read_reg ii ESP)( $\lambda original\_esp.$ 
  parT_unit(write_reg ii ESP( $original\_esp - 32w$ ))(
  parT_unit(seqT(read_reg ii EAX)( $\lambda w.$  write_m32 ii( $original\_esp - 4w$ )w))(
  parT_unit(seqT(read_reg ii ECX)( $\lambda w.$  write_m32 ii( $original\_esp - 8w$ )w))(
  parT_unit(seqT(read_reg ii EDX)( $\lambda w.$  write_m32 ii( $original\_esp - 12w$ )w))(
  parT_unit(seqT(read_reg ii EBX)( $\lambda w.$  write_m32 ii( $original\_esp - 16w$ )w))(
  parT_unit(write_m32 ii( $original\_esp - 20w$ ) $original\_esp$ )(
  parT_unit(seqT(read_reg ii EBP)( $\lambda w.$  write_m32 ii( $original\_esp - 24w$ )w))(
  parT_unit(seqT(read_reg ii ESI)( $\lambda w.$  write_m32 ii( $original\_esp - 28w$ )w))(
    (seqT(read_reg ii EDI)( $\lambda w.$  write_m32 ii( $original\_esp - 32w$ )w)))))))))
```

x86_exec_pop_eip *ii* =

```
seqT(seqT(read_reg ii ESP)( $\lambda esp.$  addT esp(write_reg ii ESP( $esp + 4w$ ))))
  ( $\lambda(old\_esp, x).$  seqT(read_m32 ii old\_esp)
    ( $\lambda w.$  write_eip ii w))
```

x86_exec_push_eip *ii* =

```
(seqT
  (parT(read_eip ii)
    (seqT(read_reg ii ESP)( $\lambda w.$  constT( $w - 4w$ ))))
  ( $\lambda(w, esp).$  parT_unit(write_m32 ii esp w)(write_reg ii ESP esp)))
```

x86_exec_call *ii imm_rm len* =

```
seqT(parT(read_reg ii ESP)
  (parT(read_eip ii)
    (ea_Ximm_rm ii imm_rm)))( $\lambda(old\_esp, (old\_eip, ea)).$ 
```

let *bumped_eip* = *old_eip* + *len* **in**

```

seqT(call_dest_from_ea ii bumped_eip ea)(λdestw.
  (parT_unit(write_m32 ii old_esp bumped_eip)
    (parT_unit(write_reg ii ESP(old_esp - 4w))
      (write_eip ii destw))))))

x86_exec_ret ii imm =
seqT(read_reg ii ESP)(λold_esp.
seqT(addT old_esp(read_m32 ii old_esp))(λ(old_esp, retw).
  parT_unit(write_reg ii ESP(old_esp + imm + 4w))
    (write_eip ii retw)))

(x86_exec ii(XBINOP binop_name ds)len = bump_eip ii len
(seqT
  (parT(read_src_ea ii ds)(read_dest_ea ii ds)
    (λ((ea_src, val_src), (ea_dest, val_dest)).
      write_binop ii binop_name val_dest val_src ea_dest))) ∧
(x86_exec ii(XMONOP monop_name rm)len = bump_eip ii len
(seqT
  (seqT(ea_Xrm ii rm)(λea. addT ea(read_ea ii ea))
    (λ(ea_dest, val_dest).
      write_monop ii monop_name val_dest ea_dest))) ∧
(x86_exec ii(XXADD rm r)len = bump_eip ii len
(seqT
  (parT(seqT(ea_Xrm ii rm)(λea. addT ea(read_ea ii ea))
    (parT(constT(XEA_R r))(read_reg ii r)))
    (λ((ea_dest, val_dest), (ea_src, val_src)).
      seqT(write_ea ii ea_src val_dest)
        (λx. write_binop ii XADD val_src val_dest ea_dest)))))) ∧
(x86_exec ii(XXCHG rm r)len =
(if rm_is_memory_access rm then lockT else I)
(bump_eip ii len
(if rm = (XR r) then constT() else
  (seqT
    (parT(seqT(ea_Xrm ii rm)(λea. addT ea(read_ea ii ea))
      (parT(constT(XEA_R r))(read_reg ii r)))
      (λ((ea_dest, val_dest), (ea_src, val_src)).
        (parT_unit(write_ea ii ea_src val_dest)
          (write_ea ii ea_dest val_src))))))))) ∧
(x86_exec ii(XCMPXCHG rm r)len = bump_eip ii len
(seqT
  (parT(seqT(ea_Xrm ii rm)(λea. addT ea(read_ea ii ea))
    (read_reg ii EAX))
    (λ((dest_ea, dest_val), acc).
      parT_unit(write_binop ii XCMP acc dest_val(XEA_R EAX))
        (if acc = dest_val then
          seqT(read_reg ii r)(λsrc_val. write_ea ii dest_ea src_val)
        else
          write_reg ii EAX dest_val)))))) ∧

```

```

(x86_exec ii(XPOP rm)len = bump_eip ii len(x86_exec_pop ii rm)) ∧
(x86_exec ii(XPUSH imm_rm)len = bump_eip ii len(x86_exec_push ii imm_rm)) ∧
(x86_exec ii(XCALL imm_rm)len = x86_exec_call ii imm_rm len) ∧
(x86_exec ii(XRET imm)len = x86_exec_ret ii imm) ∧
(x86_exec ii(XLEA ds)len = bump_eip ii len
(seqT
  ((parT(ea_Xsrc ii ds)(ea_Xdest ii ds))
    (λ(ea_src, ea_dest).
      write_ea ii ea_dest(get_ea_address ea_src)))) ∧
(x86_exec ii(XMOV c ds)len = bump_eip ii len
(seqT
  ((parT(read_src_ea ii ds)
    (parT(read_cond ii c)(ea_Xdest ii ds))))
    (λ((ea_src, val_src), (g, ea_dest)).
      if g then write_ea ii ea_dest val_src else constT())))) ∧
(x86_exec ii(XJUMP c imm)len = (
seqT
  (parT(read_eip ii)(read_cond ii c))
    (λ(eip, g). write_eip ii(if g then eip + len + imm else eip + len)))) ∧
(x86_exec ii(XLOOP c imm)len =
seqT(parT(read_eip ii)(
  parT(read_cond ii c)
    (seqT(read_reg ii ECX)(λecx. constT(ecx - 1w))))))
  (λ(eip, guard, new_ecx).
    parT_unit(write_reg ii ECX new_ecx)
      (write_eip ii
        (if ¬(new_ecx = 0w) ∧ guard
          then eip + len + imm else eip + len)))))) ∧
(x86_exec ii(XPUSHAD)len = bump_eip ii len(
x86_exec_pushad ii)) ∧
(x86_exec ii(XPOPAD)len = bump_eip ii len(
x86_exec_popad ii))

(x86_execute ii(XPREFIX XG1_NONE g2 i)len = x86_exec ii i len) ∧
(x86_execute ii(XPREFIX XLOCK g2 i)len = lockT(x86_exec ii i len))

```

Part IX
x86_decoder

```

(STR_SPACE_AUX n"" = "") ∧
(STR_SPACE_AUX n(STRING c s) =
if n = 0 then STRING#""(STRING c(STR_SPACE_AUX 1 s))
  else STRING c(STR_SPACE_AUX(n - 1)s))

```

```
bytebits = hex2bits o STR_SPACE_AUX 2
```

```

check_opcode s =
let y = (n2bits 3 o char2num o hd o TL o explode)s in
assert(λg.g"Reg/Opcode" = y)

```

```

read_SIB =
assign_drop"Base"3 >> assign_drop"Index"3 >> assign_drop"Scale"2 >>
option_try[
assert(λg.(g"Mod" = [F; F]) ∧ (g"Base" = [T; F; T])) >> assign_drop"disp32"32;
assert(λg.(g"Mod" = [F; F]) ∧ ¬(g"Base" = [T; F; T]));
assert(λg.(g"Mod" = [T; F])) >> assign_drop"disp8"8;
assert(λg.(g"Mod" = [F; T])) >> assign_drop"disp32"32]

```

```

read_ModRM =
assign_drop"R/M"3 >> assign_drop"Reg/Opcode"3 >> assign_drop"Mod"2 >>
option_try[
assert(λg.(g"Mod" = [T; T]));
assert(λg.(g"Mod" = [F; F]) ∧ ¬(g"R/M" = [F; F; T]) ∧ ¬(g"R/M" = [T; F; T]));
assert(λg.(g"Mod" = [F; F]) ∧ (g"R/M" = [T; F; T])) >> assign_drop"disp32"32;
assert(λg.(g"Mod" = [T; F]) ∧ ¬(g"R/M" = [F; F; T])) >> assign_drop"disp8"8;
assert(λg.(g"Mod" = [F; T]) ∧ ¬(g"R/M" = [F; F; T])) >> assign_drop"disp32"32;
assert(λg.¬(g"Mod" = [T; T]) ∧ (g"R/M" = [F; F; T])) >> read_SIB]

```

```
is_hex_add x = ((implode o DROP 2 o explode)x = "+rd")
```

```

process_hex_add name =
let n = (hex2num o implode o TAKE 2 o explode)name in
option_try[drop_eq(n2bits 8(n + 0)) >> assign"reg"(n2bits 3 0);
  drop_eq(n2bits 8(n + 1)) >> assign"reg"(n2bits 3 1);
  drop_eq(n2bits 8(n + 2)) >> assign"reg"(n2bits 3 2);
  drop_eq(n2bits 8(n + 3)) >> assign"reg"(n2bits 3 3);
  drop_eq(n2bits 8(n + 4)) >> assign"reg"(n2bits 3 4);
  drop_eq(n2bits 8(n + 5)) >> assign"reg"(n2bits 3 5);
  drop_eq(n2bits 8(n + 6)) >> assign"reg"(n2bits 3 6);
  drop_eq(n2bits 8(n + 7)) >> assign"reg"(n2bits 3 7)]

```



```

x86_match_step name =
if is_hex name  $\wedge$  (STRLEN name = 2) then (* opcode e.g. FE, 83 and 04 *)
  drop_eq(n2bits 8(hex2num name))
  else if is_hex_add name then (* opcode + rd, e.g. F8+rd *)
    process_hex_add name
  else if name = "1" then (* constant 1 *)
    assign_drop name 0
  else if mem name ["ib"; "cb"; "rel8"; "imm8"] then (* 8-bit immediate or address *)
    assign_drop name 8
  else if mem name ["iw"; "cw"; "imm16"] then (* 16-bit immediate or address *)
    assign_drop name 16
  else if mem name ["id"; "cd"; "rel32"; "imm32"] then (* 32-bit immediate or address *)
    assign_drop name 32
  else if name = "/r" then (* normal reg + reg/mem *)
    read_ModRM
  else if mem name ["/0"; "/1"; "/2"; "/3"; "/4"; "/5"; "/6"; "/7"] then (* opcode extension in ModRM *)
    read_ModRM  $\gg$  check_opcode name
  else
    option_fail

```

```

x86_binop =
[("ADD", XADD); ("AND", XAND); ("CMP", XCMP); ("OR", XOR); ("SAR", XSAR); ("SHR", XSHR); ("SHL", XSHL); ("SU

```

```

x86_monop =
[("DEC", XDEC); ("INC", XINC); ("NOT", XNOT); ("NEG", XNEG)]

```

```

b2reg g name = (EL(bits2num(g name)))[EAX; ECX; EDX; EBX; ESP; EBP; ESI; EDI] : Xreg

```

```

decode_Xr32 g name =
if name = "EAX" then EAX else
if g"reg" = [] then b2reg g"Reg/Opcode" else b2reg g"reg"

```

```

decode_SIB g =
let scaled_index = (if g"Index" = [F; F; T] then NONE else SOME (b2w g"Scale", b2reg g"Index")) in
if g"Base" = [T; F; T] then (* the special case indicated by "[*]" *)
  if g"Mod" = [F; F] then XM scaled_index NONE (b2w g"disp32") else
  if g"Mod" = [T; F] then XM scaled_index (SOME EBP) (b2w g"disp8") else
  (* g"Mod" = [F; T] *) XM scaled_index (SOME EBP) (b2w g"disp32")
else (* normal cases, just need to read off the correct displacement *)
  let disp = (if (g"Mod" = [T; F]) then sw2sw((b2w g"disp8") : word8) else b2w g"disp32") in
  let disp = (if (g"Mod" = [F; F]) then 0w else disp) in
  XM scaled_index (SOME (b2reg g"Base")) disp

```

```

decode_Xrm32 g name =
if name = "EAX" then XR EAX else
if (g"Mod" = [F; F])  $\wedge$  (g"R/M" = [T; F; T]) then XM NONE NONE (b2w g"disp32") else

```

```

if  $\neg$ ( $g$ “Mod” = [T; T])  $\wedge$  ( $g$ “R/M” = [F; F; T]) then decode_SIB  $g$  else
if ( $g$ “Mod” = [F; F]) then XM NONE(SOME (b2reg  $g$ “R/M”))0w else
if ( $g$ “Mod” = [T; F]) then XM NONE(SOME (b2reg  $g$ “R/M”))(sw2sw : word8  $\rightarrow$  word32(b2w  $g$ “disp8”)) else
if ( $g$ “Mod” = [F; T]) then XM NONE(SOME (b2reg  $g$ “R/M”))(b2w  $g$ “disp32”) else
if ( $g$ “Mod” = [T; T]) then XR(b2reg  $g$ “R/M”) else XR(b2reg  $g$ “reg”)

```

```

decode_Xconst name  $g$  =
if name = “imm8” then sw2sw : word8  $\rightarrow$  word32(b2w  $g$ “ib”) else
if name = “rel8” then sw2sw : word8  $\rightarrow$  word32(b2w  $g$ “cb”) else
if name = “imm16” then sw2sw : word16  $\rightarrow$  word32(b2w  $g$ “iw”) else
if name = “imm32” then b2w  $g$ “id” else
if name = “rel32” then b2w  $g$ “cd” else
if name = “1” then 1w else 0w

```

```

decode_Xdest_src  $g$  dest src =
if src = “r32” then XRM_R(decode_Xrm32  $g$  dest)(decode_Xr32  $g$  src) else
if src = “r/m32” then XR_RM(decode_Xr32  $g$  dest)(decode_Xrm32  $g$  src) else
if src = “m” then XR_RM(decode_Xr32  $g$  dest)(decode_Xrm32  $g$  src) else
  XRM_I(decode_Xrm32  $g$  dest)(decode_Xconst src  $g$ )

```

```

decode_Xconst_or_zero ts  $g$  =
if length ts < 2 then 0w else decode_Xconst(EL 1 ts) $g$ 

```

```

decode_Ximm_rm ts  $g$  =
if mem (EL 1 ts) [“r/m32”; “r32”]
then XLRM(decode_Xrm32  $g$ (EL 1 ts))
else Xi(decode_Xconst(EL 1 ts) $g$ )

```

```

x86_select_op name list = snd(hd(filter( $\lambda x$ . fst x = name)list))

```

```

X_SOME  $f$  = SOME o( $\lambda(g, w)$ .( $f$   $g$ ,  $w$ ))

```

```

x86_syntax ts =
if length ts = 0 then option_fail else
if mem (hd ts) (map fst x86_binop) then X_SOME( $\lambda g$ . $\hat{\ }x86\_syntax\_binop$ ) else
if mem (hd ts) (map fst x86_monop) then X_SOME( $\lambda g$ . $\hat{\ }x86\_syntax\_monop$ ) else
if hd ts = “POP” then X_SOME( $\lambda g$ .XPOP(decode_Xrm32  $g$ (EL 1 ts))) else
if hd ts = “PUSH” then X_SOME( $\lambda g$ .XPUSH(decode_Ximm_rm ts  $g$ )) else
if hd ts = “PUSHAD” then X_SOME( $\lambda g$ .XPUSHAD) else
if hd ts = “POPAD” then X_SOME( $\lambda g$ .XPOPAD) else
if hd ts = “CMPXCHG” then X_SOME( $\lambda g$ .XCMPXCHG(decode_Xrm32  $g$ (EL 1 ts))(decode_Xr32  $g$ (EL 2 ts))) else
if hd ts = “XCHG” then X_SOME( $\lambda g$ .XXCHG(decode_Xrm32  $g$ (EL 1 ts))(decode_Xr32  $g$ (EL 2 ts))) else
if hd ts = “XADD” then X_SOME( $\lambda g$ .XXADD(decode_Xrm32  $g$ (EL 1 ts))(decode_Xr32  $g$ (EL 2 ts))) else
if hd ts = “JMP” then X_SOME( $\lambda g$ .XJUMP X_ALWAYS(decode_Xconst_or_zero ts  $g$ )) else
if hd ts = “JE” then X_SOME( $\lambda g$ .XJUMP X_E(decode_Xconst_or_zero ts  $g$ )) else

```

```

if hd ts = "JNE" then X_SOME( $\lambda g$ .XJUMP X_NE(decode_Xconst_or_zero ts g)) else
if hd ts = "LEA" then X_SOME( $\lambda g$ .XLEA(decode_Xdest_src g(EL 1 ts)(EL 2 ts))) else
if hd ts = "LOOP" then X_SOME( $\lambda g$ .XLOOP X_ALWAYS(decode_Xconst_or_zero ts g)) else
if hd ts = "LOOPE" then X_SOME( $\lambda g$ .XLOOP X_E(decode_Xconst_or_zero ts g)) else
if hd ts = "LOOPNE" then X_SOME( $\lambda g$ .XLOOP X_NE(decode_Xconst_or_zero ts g)) else
if hd ts = "MOV" then X_SOME( $\lambda g$ .XMOV X_ALWAYS(decode_Xdest_src g(EL 1 ts)(EL 2 ts))) else
if hd ts = "CMOVE" then X_SOME( $\lambda g$ .XMOV X_E(decode_Xdest_src g(EL 1 ts)(EL 2 ts))) else
if hd ts = "CMOVNE" then X_SOME( $\lambda g$ .XMOV X_NE(decode_Xdest_src g(EL 1 ts)(EL 2 ts))) else
if hd ts = "CALL" then X_SOME( $\lambda g$ .XCALL(decode_Ximm_rm ts g)) else
if hd ts = "RET" then X_SOME( $\lambda g$ .XRET(decode_Xconst_or_zero ts g)) else option_fail

```

```

x86_decode_aux = (match_list x86_match_step tokenise(x86_syntax o tokenise) o
  map( $\lambda s$ .let x = STR_SPLIT["#"]s in (EL 0 x, EL 1 x)) ^ x86_syntax_list

```

```

x86_decode_prefixes w =
if length w < 16 then (XG1_NONE, XG2_NONE, w) else
let bt1 = (TAKE 8 w = n2bits 8(hex2num"2E")) in
let bnt1 = (TAKE 8 w = n2bits 8(hex2num"3E")) in
let l1 = (TAKE 8 w = n2bits 8(hex2num"F0")) in
let bt2 = (TAKE 8(DROP 8 w) = n2bits 8(hex2num"2E"))  $\wedge$  l1 in
let bnt2 = (TAKE 8(DROP 8 w) = n2bits 8(hex2num"3E"))  $\wedge$  l1 in
let l2 = (TAKE 8(DROP 8 w) = n2bits 8(hex2num"F0"))  $\wedge$  (bt1  $\vee$  bnt1) in
let g1 = if l1  $\vee$  l2 then XLOCK else XG1_NONE in
let g2 = if bt1  $\vee$  bt2 then XBRANCH_TAKEN else XG2_NONE in
let g2 = if bnt1  $\vee$  bnt2 then XBRANCH_NOT_TAKEN else g2 in
let n = if bt1  $\vee$  bnt1  $\vee$  l1 then (if bt2  $\vee$  bnt2  $\vee$  l2 then 16 else 8) else 0 in
  (g1, g2, DROP n w)

```

```

(dest_accesses_memory(XRM_I rm i) = rm_is_memory_access rm)  $\wedge$ 
(dest_accesses_memory(XRM_R rm r) = rm_is_memory_access rm)  $\wedge$ 
(dest_accesses_memory(XR_RM r rm) = F)

```

```

(x86_lock_ok(XBINOP binop_name ds) =
mem binop_name [XADD; XAND; XOR; XSUB; XXOR]  $\wedge$ 
dest_accesses_memory ds)  $\wedge$ 
(x86_lock_ok(XMONOP monop_name rm) =
mem monop_name [XDEC; XINC; XNEG; XNOT]  $\wedge$ 
rm_is_memory_access rm)  $\wedge$ 
(x86_lock_ok(XXADD rm r) = rm_is_memory_access rm)  $\wedge$ 
(x86_lock_ok(XXCHG rm r) = rm_is_memory_access rm)  $\wedge$ 
(x86_lock_ok(XCMPXCHG rm r) = rm_is_memory_access rm)  $\wedge$ 
(x86_lock_ok(XPOP rm) = F)  $\wedge$ 
(x86_lock_ok(XLEA ds) = F)  $\wedge$ 
(x86_lock_ok(XPUSH imm_rm) = F)  $\wedge$ 
(x86_lock_ok(XCALL imm_rm) = F)  $\wedge$ 
(x86_lock_ok(XRET imm) = F)  $\wedge$ 
(x86_lock_ok(XMOV c ds) = F)  $\wedge$ 

```

$(\text{x86_lock_ok}(\text{XJUMP } c \text{ imm}) = \mathbf{F}) \wedge$
 $(\text{x86_lock_ok}(\text{XLOOP } c \text{ imm}) = \mathbf{F}) \wedge$
 $(\text{x86_lock_ok}(\text{XPUSHAD}) = \mathbf{F}) \wedge$
 $(\text{x86_lock_ok}(\text{XPOPAD}) = \mathbf{F})$

$\text{x86_decode } w =$
let $(g1, g2, w) = \text{x86_decode_prefixes } w$ **in**
let $\text{result} = \text{x86_decode_aux } w$ **in**
if $\text{result} = \text{NONE}$ **then** NONE **else**
 let $(i, w) = \text{the result in}$
 if $\neg(g1 = \text{XLOCK}) \vee \text{x86_lock_ok } i$ **then** $\text{SOME } (\text{XPREFIX } g1 \text{ } g2 \text{ } i, w)$ **else** NONE

$\text{x86_decode_bytes } b = \text{x86_decode}(\text{FOLDR[]} @ (\text{map } w2bits \text{ } b))$

$(\text{rm_args_ok}(\text{XR } r) = \mathbf{T}) \wedge$
 $(\text{rm_args_ok}(\text{XM NONE NONE } t3) = \mathbf{T}) \wedge$
 $(\text{rm_args_ok}(\text{XM NONE } (\text{SOME } br) t3) = \mathbf{T}) \wedge$
 $(\text{rm_args_ok}(\text{XM } (\text{SOME } (s, ir)) \text{ NONE } t3) = \neg(ir = \text{ESP})) \wedge$
 $(\text{rm_args_ok}(\text{XM } (\text{SOME } (s, ir)) (\text{SOME } br) t3) = \neg(ir = \text{ESP}))$

$(\text{dest_src_args_ok}(\text{XRM_I } rm \text{ } i) = \text{rm_args_ok } rm) \wedge$
 $(\text{dest_src_args_ok}(\text{XRM_R } rm \text{ } r) = \text{rm_args_ok } rm) \wedge$
 $(\text{dest_src_args_ok}(\text{XR_RM } r \text{ } rm) = \text{rm_args_ok } rm)$

$(\text{imm_rm_args_ok}(\text{XLRM } rm) = \text{rm_args_ok } rm) \wedge$
 $(\text{imm_rm_args_ok}(\text{XI } i) = \mathbf{T})$

$(\text{x86_args_ok}(\text{XBINOP } binop_name \text{ } ds) = \text{dest_src_args_ok } ds) \wedge$
 $(\text{x86_args_ok}(\text{XMONOP } monop_name \text{ } rm) = \text{rm_args_ok } rm) \wedge$
 $(\text{x86_args_ok}(\text{XXADD } rm \text{ } r) = \text{rm_args_ok } rm) \wedge$
 $(\text{x86_args_ok}(\text{XXCHG } rm \text{ } r) = \text{rm_args_ok } rm) \wedge$
 $(\text{x86_args_ok}(\text{XCMPXCHG } rm \text{ } r) = \text{rm_args_ok } rm) \wedge$
 $(\text{x86_args_ok}(\text{XPOP } rm) = \text{rm_args_ok } rm) \wedge$
 $(\text{x86_args_ok}(\text{XPUSH } imm_rm) = \text{imm_rm_args_ok } imm_rm) \wedge$
 $(\text{x86_args_ok}(\text{XCALL } imm_rm) = \text{imm_rm_args_ok } imm_rm) \wedge$
 $(\text{x86_args_ok}(\text{XRET } imm) = \mathbf{w2n } imm < 2 * *16) \wedge$
 $(\text{x86_args_ok}(\text{XMOV } c \text{ } ds) = \text{dest_src_args_ok } ds \wedge \mathbf{mem } c [\text{X_NE}; \text{X_E}; \text{X_ALWAYS}]) \wedge (* \text{ partial list } *)$
 $(\text{x86_args_ok}(\text{XJUMP } c \text{ } imm) = \mathbf{F}) \wedge$
 $(\text{x86_args_ok}(\text{XLOOP } c \text{ } imm) = \mathbf{mem } c [\text{X_NE}; \text{X_E}; \text{X_ALWAYS}]) \wedge$
 $(\text{x86_args_ok}(\text{XPUSHAD}) = \mathbf{T}) \wedge$
 $(\text{x86_args_ok}(\text{XPOPAD}) = \mathbf{T})$

$(\text{x86_well_formed_instruction}(\text{XPREFIX XLOCK } g2 \text{ } i) = \text{x86_lock_ok } i \wedge \text{x86_args_ok } i) \wedge$
 $(\text{x86_well_formed_instruction}(\text{XPREFIX XG1_NONE } g2 \text{ } i) = \text{x86_args_ok } i)$

Part X

x86_

```
iiid_dummy = { proc := 0; program_order_index := 0 }
```

```
x86_execute_some i w s = option_apply(x86_execute iiid_dummy i w s)(λt.SOME (snd t))
```

```
X86_NEXT s =
```

```
let e = XREAD_EIP s in (* read eip *)
```

```
let xs = map the(XREAD_MEM_BYTES 20 e s) in (* read next 20 bytes *)
```

```
let m = x86_decode_bytes xs in (* attempt to decode *)
```

```
if m = NONE then NONE else (* if decoded fail, return NONE *)
```

```
  let (i, w) = the m in (* otherwise extract content *)
```

```
  let n = 20 - (length w div 8) in (* calc length of instruction *)
```

```
    if every(λx.¬(x = NONE))(XREAD_MEM_BYTES n e s)(* check that the memory is there *)
```

```
      then x86_execute_some i(n2w n)s else NONE(* execute the instruction *)
```

Part XI
x86_program

DOMAIN $f = \{x \mid \neg(f\ x = \text{NONE})\}$

type_abbrev program_word8 : (address \rightarrow word8 option)

type_abbrev program_Xinst : (address \rightarrow (Xinst#num) option)

read_mem_bytes $n\ a\ m =$

if $n = 0$ **then** [] **else** $m\ a \in \text{read_mem_bytes}(n - 1)(a + 1w)m$

(decode_program_fun : program_word8 \rightarrow address \rightarrow (Xinst#num) option) prog_word8 $a =$

let $xs = \text{map the}(\text{read_mem_bytes}\ 20\ a\ \text{prog_word8})$ **in** (* read next 20 bytes *)

let $\text{decode} = \text{x86_decode_bytes}\ xs$ **in** (* attempt to decode *)

case decode **of**

NONE \rightarrow NONE (* if decoding fails, then fail *)

|| SOME $(i, w) \rightarrow$ (* otherwise extract content *)

let $n = 20 - (\text{length}\ w\ \text{div}\ 8)$ **in** (* calc length of instruction *)

if **every** $(\lambda x. \neg(x = \text{NONE}))(\text{read_mem_bytes}\ n\ a\ \text{prog_word8})$ (* check the memory is there *)

then SOME (i, n)

else NONE

(decode_program_rel : program_word8 \rightarrow program_Xinst \rightarrow bool)

 prog_word8 prog_Xinst =

$\forall a.$ **case** prog_Xinst a **of**

 NONE \rightarrow **T**

 || SOME $(inst, n) \rightarrow \text{decode_program_fun}\ \text{prog_word8}\ a = \text{SOME}\ (inst, n)$

type_abbrev run_skeleton : (proc \rightarrow (program_order_index \rightarrow address option))

(run_skeleton_wf : address set \rightarrow run_skeleton \rightarrow bool) $addr\ rs =$

$(\forall p\ i\ i'. ((\neg((rs\ p\ i') = \text{NONE})) \wedge (i < i')) \implies (\neg((rs\ p\ i) = \text{NONE}))) \wedge$

$(\forall p\ i\ a. (rs\ p\ i = \text{SOME}\ a) \implies a \in \text{addr}) \wedge$

finite $\{p \mid \exists i\ a. rs\ p\ i = \text{SOME}\ a\}$

x86_event_execute = x86_event_opsem \$x86_execute

x86_execute_with_eip_check $ii\ inst\ len\ eip =$

let $s = (\text{x86_event_execute}\ ii\ inst\ len)\{\}$ **in**

 { E

 | $\exists eiid_next\ x.$

$(eiid_next, x, E) \in s \wedge$

$\forall v\ ev. ((ev.action = (\text{ACCESS}\ R(\text{LOCATION_REG}\ ii.\text{proc}\ \text{REG_EIP})v)) \wedge$

$ev \in E.events) \implies (v = eip)$

 }


```

(event_structures_of_run_skeleton : program_Xinst → run_skeleton → event_structure set)
  prog_Xinst rs =
let Ess = {x86_execute_with_eip_check(⟦ proc := p; program_order_index := i ⟧ inst(n2w n) eip |
  (rs p i = SOME eip) ∧ (SOME (inst, n) = prog_Xinst eip))}
in
{event_structure_bigunion Es | Es ∈ all_choices Ess}

(x86_semantics : program_word8 → state_constraint →
(run_skeleton#program_Xinst#((event_structure#(execution_witness set))set))set)
prog_word8 initial_state =

let x1 = {(rs, prog_Xinst) | rs, prog_Xinst | run_skeleton_wf(DOMAIN prog_Xinst)rs ∧
  decode_program_rel prog_word8 prog_Xinst} in

let x2 = {(rs, prog_Xinst, Es) | (rs, prog_Xinst) ∈ x1 ∧
  (Es = event_structures_of_run_skeleton prog_Xinst rs)} in

let x3 = {(rs, prog_Xinst, {(E, Xs) | E ∈ Es ∧
  (Xs = {X | valid_execution E X ∧
  (X.initial_state = initial_state))})}
  | (rs, prog_Xinst, Es) ∈ x2} in
x3

(lts_po_of_event_structure (* : event_structure -> (event set,unit,machine_visible_label) LTS *)E =
⟦ states := POW E.events;
  initial := {};
  final := if finite E.events then {(E.events, ())} else {};
  trans := {(s, (VIS(⟦ mvl_event := e;
    mvl_iico := {e' | e' ∈ s ∧ (e', e) ∈ E.intra_causality};
    mvl_first_of_instruction := ¬(∃(e' ∈ s). e'.iuid = e.iuid);
    mvl_last_of_instruction := ¬(∃(e' ∈ (E.events \ s)). e'.iuid = e.iuid);
    mvl_locked := locked E e
  ⟧)), s ∪ {e}) | e ∈ E.events ∧ ¬(e ∈ s) ∧
  e ∈ minimal_elements(E.events \ s)(po_iico E)} ⟧

```

Part XII

x86_sequential_axiomatic_model

sequential_execution E $so =$
 linear_order so $E.events$ \wedge
 $(\forall(es \in (E.atomicity))(e_1 \in es)(e_2 \in es)e.$
 $(e_1, e) \in so \wedge (e, e_2) \in so \implies e \in es)$

so_to_vo E $so = \lambda p.$ **if** $p \in E.procs$ **then** $so|_{(viewed_events\ E\ p)}$ **else** $\{\}$

so_to_write_serialization $so =$
 $\{(e_1, e_2) \mid (e_1, e_2) \in (strict\ so) \wedge mem_store\ e_1 \wedge mem_store\ e_2 \wedge (loc\ e_1 = loc\ e_2)\}$

so_to_lock_serialization E $so =$
 $\{(e_1, e_2) \mid (e_1, e_2) \in (strict\ so) \wedge$
 $\exists es_1\ es_2 \in (E.atomicity). \neg(es_1 = es_2) \wedge e_1 \in es_1 \wedge e_2 \in es_2\}$

so_to_rfmap E $so =$
 $\{(ew, er) \mid (ew, er) \in so \wedge ew \in (writes\ E) \wedge er \in (reads\ E) \wedge (loc\ er = loc\ ew) \wedge$
 $(\forall ew' \in (writes\ E). \neg(ew = ew') \wedge (ew, ew') \in so \wedge (ew', er) \in so$
 \implies
 $\neg(loc\ ew = loc\ ew'))\}$

so_to_exec_witness E $initial_state$ $so =$
 $\langle\langle$ $initial_state := initial_state;$
 $vo := so_to_vo\ E\ so;$
 $write_serialization := so_to_write_serialization\ so;$
 $lock_serialization := so_to_lock_serialization\ E\ so;$
 $rfmap := so_to_rfmap\ E\ so\rangle\rangle$

valid_sequential_execution E $initial_state$ $so =$
 sequential_execution E so \wedge
 valid_execution $E(so_to_exec_witness\ E\ initial_state\ so)$

competes E $X =$
 $\{(e_1, e_2) \mid \neg(e_1 = e_2) \wedge (loc\ e_1 = loc\ e_2) \wedge$
 $((e_1 \in writes\ E \wedge mem_store\ e_1 \wedge e_2 \in reads\ E) \vee$
 $(e_2 \in writes\ E \wedge mem_store\ e_2 \wedge e_1 \in reads\ E))\}$
 $\setminus ((happens_before\ E\ X)^+ \cup ((happens_before\ E\ X)^+)^{-1})$

race_free E $X = \forall e_1\ e_2 \in (E.events).$
 $\neg((e_1, e_2) \in competes\ E\ X)$

restrictE E $es =$
 $\langle\langle$ $procs := E.procs;$
 $events := E.events \cap es;$
 $intra_causality := E.intra_causality|_{es};$
 $atomicity := PER_RESTRICT\ E.atomicity\ es\rangle\rangle$

$\text{prefixes } E X = \{E' \mid \text{sub_event_structure } E' E \wedge \forall e_1 e_2.$
 $e_2 \in E'.\text{events} \wedge (e_1, e_2) \in (\text{happens_before } E X) \implies$
 $e_1 \in E'.\text{events}\}$

$\text{sequential_race_free } E X = \forall (E' \in (\text{prefixes } E X)) \text{so.}$
 $\text{valid_sequential_execution } E' X.\text{initial_state so} \implies$
 $\forall e_1 e_2. \neg((e_1, e_2) \in \text{competes } E'$
 $(\text{so_to_exec_witness } E' X.\text{initial_state so}))$

Part XIII

x86_drf

$wfes\ E =$
 $(\forall iid.\mathbf{finite}\{e_{iid} \mid \exists e \in (E.events).(e.iid = iid) \wedge (e.eiid = eiid)\}) \wedge$
 $(\mathbf{finite}\ E.procs) \wedge$
 $(\forall e \in (E.events).\mathbf{proc}\ e \in E.procs) \wedge$
 $(\forall e_1\ e_2 \in (E.events).(e_1.eiid = e_2.eiid) \wedge (e_1.iid = e_2.iid) \implies (e_1 = e_2)) \wedge$
 $(DOM\ E.intra_causality) \subseteq E.events \wedge$
 $(\mathbf{range}\ E.intra_causality) \subseteq E.events \wedge$
 $\mathbf{acyclic}(E.intra_causality) \wedge$
 $(\forall (e_1, e_2) \in (E.intra_causality).(e_1.iid = e_2.iid)) \wedge$
 $(\forall (e_1 \in \mathbf{writes}\ E)\ e_2.$
 $\neg(e_1 = e_2) \wedge$
 $(e_2 \in \mathbf{writes}\ E \vee e_2 \in \mathbf{reads}\ E)) \wedge$
 $(e_1.iid = e_2.iid) \wedge$
 $(\mathbf{loc}\ e_1 = \mathbf{loc}\ e_2) \wedge$
 $(\exists p\ r.\mathbf{loc}\ e_1 = \mathbf{SOME}\ (\mathbf{LOCATION_REG}\ p\ r))$
 \implies
 $(e_1, e_2) \in E.intra_causality^+ \vee$
 $(e_2, e_1) \in E.intra_causality^+) \wedge$
 $PER\ E.events\ E.atomicity \wedge$
 $(\forall es \in (E.atomicity).\forall e_1\ e_2 \in es.(e_1.iid = e_2.iid)) \wedge$
 $(\forall es \in (E.atomicity).\forall e_1 \in es.\forall e_2 \in (E.events).(e_1.iid = e_2.iid) \implies e_2 \in es) \wedge$
 $(\forall e \in (E.events).\forall p\ r.(\mathbf{loc}\ e = \mathbf{SOME}\ (\mathbf{LOCATION_REG}\ p\ r)) \implies (p = \mathbf{proc}\ e))$

$\mathbf{maximal_es}\ E\ X = \mathbf{maximal_elements}\ E.events(\mathbf{happens_before}\ E\ X)$

$\mathbf{deleteE}\ E\ e =$
 $\langle\langle\ \mathbf{procs} := E.procs;$
 $\ \mathbf{events} := E.events\ \mathbf{DELETE}\ e;$
 $\ \mathbf{intra_causality} := E.intra_causality|_{(E.events\ \mathbf{DELETE}\ e)};$
 $\ \mathbf{atomicity} := PER_RESTRICT\ E.atomicity(E.events\ \mathbf{DELETE}\ e)\ \rangle\rangle$

$\mathbf{extend_so}\ E\ so\ e =$
 $so \cup \{(e_1, e) \mid e_1 \mid e_1 \in E.events\}$

$\mathbf{locked_ready}\ E\ X\ es =$
 $\forall e\ e'.e \in es \wedge (e, e') \in \mathbf{happens_before}\ E\ X \implies e' \in es$

$\mathbf{ind_hyp1}\ E\ X\ so =$
 $\forall es\ e.$
 $es \in E.atomicity \wedge$
 $(\exists e'.e' \in es \wedge \mathbf{locked_ready}\ E\ X\ es) \wedge$
 $e \in \mathbf{maximal_elements}\ E.events\ so$
 \implies
 $e \in es$

sequential_order_thm =
 $\forall E X. \text{wfes } E \wedge \mathbf{finite} E.\text{events} \wedge$
 $\text{race_free } E X \wedge \text{valid_execution } E X$
 $\implies \exists so.$
 $\text{valid_sequential_execution } E X.\text{initial_state } so \wedge$
 $\text{ind_hyp1 } E X so \wedge$
 $(\text{happens_before } E(\text{so_to_exec_witness } E X.\text{initial_state } so))$
 $\subseteq (\text{strict } so) \wedge$
 $(X.\text{write_serialization} = \text{so_to_write_serialization } so) \wedge$
 $(X.\text{lock_serialization} = \text{so_to_lock_serialization } E so) \wedge$
 $(X.\text{rfmap} = \text{so_to_rfmap } E so)$

$\text{pre } E X es = \text{restrictE } E(\mathbf{biginter}\{E''.\text{events} \mid E'' \mid es \subseteq E''.\text{events} \wedge E'' \in \text{prefixes } E X\})$

$\text{ind_concl } E' X' so =$
 $\text{valid_sequential_execution } E' X'.\text{initial_state } so \wedge$
 $(\text{happens_before } E'(\text{so_to_exec_witness } E' X'.\text{initial_state } so)) \subseteq (\text{strict } so) \wedge$
 $(X'.\text{write_serialization} = \text{so_to_write_serialization } so) \wedge$
 $(X'.\text{lock_serialization} = \text{so_to_lock_serialization } E' so) \wedge$
 $(X'.\text{rfmap} = \text{so_to_rfmap } E' so)$

$\text{ind_concl2 } E' X' so = \text{ind_concl } E' X' so \wedge \text{ind_hyp1 } E' X' so$

$\text{ind_assum } E E' X' =$
 $\mathbf{card} E'.\text{events} < \mathbf{card} E.\text{events} \wedge$
 $\text{wfes } E' \wedge$
 $\mathbf{finite} E'.\text{events} \wedge$
 $\text{sequential_race_free } E' X' \wedge$
 $\text{valid_execution } E' X'$

data_race_free_thm =
 $\forall E X. \text{well_formed_event_structure } E \wedge \mathbf{finite} E.\text{events} \wedge$
 $\text{sequential_race_free } E X \wedge \text{valid_execution } E X$
 \implies
 $\text{race_free } E X \wedge \exists so.$
 $\text{valid_sequential_execution } E X.\text{initial_state } so \wedge$
 $\text{ind_hyp1 } E X so \wedge$
 $(\text{happens_before } E(\text{so_to_exec_witness } E X.\text{initial_state } so))$
 $\subseteq (\text{strict } so) \wedge$
 $(X.\text{write_serialization} = \text{so_to_write_serialization } so) \wedge$
 $(X.\text{lock_serialization} = \text{so_to_lock_serialization } E so) \wedge$
 $(X.\text{rfmap} = \text{so_to_rfmap } E so)$

Part XIV
x86_hb_machine

clause_name $x = \mathbf{T}$

$f \oplus (x \mapsto y) = \lambda x'. \mathbf{if} \ x' = x \ \mathbf{then} \ y \ \mathbf{else} \ f \ x'$

funupd2 $f \ w \ x \ y = f \oplus (w \mapsto ((f \ w) \oplus (x \mapsto y)))$

linear_order_extend $r \ y = r \cup \{(x, y) \mid (x, x) \in r\}$

type_abbrev message : (event#address#value#(event set))

type_abbrev machine_state :

(*E*)event_structure#
 (*M*)(proc → address → (value#(event option)) option)#
 (*F*)(proc → proc → message list)#
 (*G*)(address → event list)#
 (* TODO: now we're using X, instead of having an erasure property, maybe we should lose the explicit G? *)
 (*Rg*)(proc → reg → (value#(event option)) option)#
 (*X*)execution_witness

(initial_machine_state : state_constraint → machine_state)initialstate =
 (⟦ events := {}; intra_causality := {}; atomicity := {} ⟧,
 (λp.λa.case initialstate(LOCATION_MEM a) of NONE → NONE || SOME v → SOME (v, NONE)),
 (λp1.λp2.NIL),
 (λa.NIL),
 (λp.λr.case initialstate(LOCATION_REG p r) of NONE → NONE || SOME v → SOME (v, NONE)),
 (⟦ initial_state := initialstate;
 vo := λp.{ };
 write_serialization := {};
 lock_serialization := {};
 rfmap := {} ⟧
)

execution_witness_of_machine_state($E, \mathbf{M}, \mathbf{F}, G, Rg, X$) = X

event_set_of_machine_state($E, \mathbf{M}, \mathbf{F}, G, Rg, X$) = $E.events$

next_eiid_es $E \ e = \text{next_eiid}\{e.eiid \mid e \in E.events\}$

(*****)

(* enqueueing sub-writes *)
 (∀P M F G Rg e F' a v p E X (X' : execution_witness))iico mvl.
 (clause_name “enqueue-mem-write” ∧
 (e = mvl.mvl_event) ∧

```

(iico = mvl.mvliico) ∧
(e.action = ACCESS W(LOCATION_MEM a)v) ∧
(p = e.iid.proc) ∧
(∀q.q ∈ P ⇒ ((F' p q) = [(e, a, (v, iico))] + +(F p q)))) ∧
(∀p' q.p' ∈ P ⇒ q ∈ P ⇒ ¬(p = p') ⇒ (F' p' q = F p' q)) ∧
(X' = X)
) ⇒
machine_trans P(E, M, F, G, Rg, X)(VIS mvl)(E, M, F', G, Rg, X')
) ∧

```

(*****)

```

(* Read own memory *)
(∀P M F G Rg e a v p E E' X X' eo iico mvl.
 (clause_name "mem-read" ∧
 (e = mvl.mvl_event) ∧
 (iico = mvl.mvliico) ∧
 (e.action = ACCESS R(LOCATION_MEM a)v) ∧
 (p = e.iid.proc) ∧
 (M p a = SOME (v, eo)) ∧
 (¬∃e' v' iico'. mem (e', a, v', iico') (F p p)) ∧
 (E' = [ events := E.events ∪ {e};
   intra_causality := E.intra_causality ∪ {(e', e) | e' ∈ iico};
   atomicity := E.atomicity] ) ∧
 (X' = X [ vo := X.vo ⊕ (p ↦ (linear_order_extend(X.vo p) e));
   rfmap := case eo of NONE → X.rfmap
   || SOME ew → X.rfmap ∪ {(ew, e)} ] ) ∧
 (* TODO: would it be cleaner to pull eo from the most recent write in our X.vo p, instead of recording eo in M?*)
 (∀e'.(e', e) ∈ (happens_before E' X')+ ⇒ e' ∈ viewed_events E' p ⇒ (e', e') ∈ X.vo p)
 ) ⇒
 machine_trans P(E, M, F, G, Rg, X)(VIS mvl)(E', M, F, G, Rg, X')
 ) ∧
 (*****)

```

```

(* delivering sub-writes, case (1), where iid has already been seen by *)
(* Ga (and no subwrite of a Ga-older iid is pending for this processor) *)
(∀P M F G Rg M' F' p q e a v G0 G1 E X X' iico.
 ((clause_name "deliver-mem-write-1" ∧
 (e.action = ACCESS W(LOCATION_MEM a)v) ∧
 (F = funupd2 F' p q([(F' p q) + +[(e, a, (v, iico))]])) ∧
 (G a = (G0 + +[e] + +G1)) ∧
 (∀p' e' v'.p' ∈ P ⇒ mem (e', a, v') (F p' q) ⇒ ¬(mem e' G1)) ∧
 (M' = funupd2 M q a(SOME (v, SOME e))) ∧
 (X' = X [ vo := X.vo ⊕ (q ↦ (linear_order_extend(X.vo q) e)) ] ) ∧
 (∀e'.(e', e) ∈ (happens_before E X')+ ⇒ e' ∈ viewed_events E q ⇒ (e', e') ∈ X.vo q)
 ) ⇒
 machine_trans P(E, M, F, G, Rg, X)TAU(E, M', F', G, Rg, X')
 ) ∧

```

```

(*****)

( $\forall P M \mathbf{F} G Rg M' F' G' p q a e v E E' X X' iico.$ 
  ((clause_name "deliver-mem-write-2")  $\wedge$ 
   ( $e.action = \text{ACCESS W}(\text{LOCATION\_MEM } a)v$ )  $\wedge$ 
   ( $\mathbf{F} = \text{funupd2 } F' p q((F' p q) ++ ((e, a, (v, iico))))$ )  $\wedge$ 
   ( $\neg(\text{mem } e (G a))$ )  $\wedge$ 
   ( $G' = G \oplus (a \mapsto ([e] ++ G a))$ )  $\wedge$ 
   ( $\forall p' e' v'. p' \in P \implies \text{mem } (e', a, v') (\mathbf{F} p' q) \implies \neg(\text{mem } e' (G a))$ )  $\wedge$ 
   ( $M' = \text{funupd2 } M q a(\text{SOME } (v, \text{SOME } e))$ )  $\wedge$ 
   ( $E' = \llbracket \text{events} := E.events \cup \{e\};$ 
      $\text{intra\_causality} := E.intra\_causality \cup \{(e', e) \mid e' \in iico\};$ 
      $\text{atomicity} := E.atomicity \rrbracket$ )  $\wedge$ 
   ( $X' = X \llbracket \text{vo} := X.vo \oplus (q \mapsto (\text{linear\_order\_extend}(X.vo q)e));$ 
      $\text{write\_serialization} := X.write\_serialization \cup \{(e', e) \mid \text{mem } e' (G a)\}$ )  $\wedge$ 
   ( $\forall e'. (e', e) \in (\text{happens\_before } E X')^+ \implies e' \in \text{viewed\_events } E q \implies (e', e) \in (X.vo q)$ 
   )  $\implies$ 
  machine_trans P(E, M,  $\mathbf{F}$ , G, Rg, X)TAU(E', M', F', G', Rg, X')
  )  $\wedge$ 

```

```

(*****)

( $\forall P M \mathbf{F} G Rg e r v p E E' X X' eo iico mvl.$ 
  (clause_name "reg-read"  $\wedge$ 
   ( $e = mvl.mvl\_event$ )  $\wedge$ 
   ( $iico = mvl.mvl\_iico$ )  $\wedge$ 
   ( $e.action = \text{ACCESS R}(\text{LOCATION\_REG } p r)v$ )  $\wedge$ 
   ( $Rg p r = \text{SOME } (v, eo)$ )  $\wedge$ 
   ( $E' = \llbracket \text{events} := E.events \cup \{e\};$ 
      $\text{intra\_causality} := E.intra\_causality \cup \{(e', e) \mid e' \in iico\};$ 
      $\text{atomicity} := E.atomicity \rrbracket$ )  $\wedge$ 
   ( $X' = X \llbracket \text{vo} := X.vo \oplus (p \mapsto (\text{linear\_order\_extend}(X.vo p)e);$ 
      $\text{rfmap} := \text{case } eo \text{ of NONE} \rightarrow X.\text{rfmap}$ 
      $\parallel \text{SOME } ew \rightarrow X.\text{rfmap} \cup \{(ew, e)\}$ )  $\wedge$ 
   ( $\forall e'. (e', e) \in (\text{happens\_before } E' X')^+ \implies e' \in \text{viewed\_events } E' p \implies (e', e) \in X.vo p$ 
   )  $\implies$ 
  machine_trans P(E, M,  $\mathbf{F}$ , G, Rg, X)(VIS mvl)(E', M,  $\mathbf{F}$ , G, Rg, X')
  )  $\wedge$ 

```

```

(*****)

( $\forall P M \mathbf{F} G Rg Rg' e r v p E E' X X' iico mvl.$ 
  (clause_name "reg-write"  $\wedge$ 
   ( $e = mvl.mvl\_event$ )  $\wedge$ 
   ( $iico = mvl.mvl\_iico$ )  $\wedge$ 
   ( $e.action = \text{ACCESS W}(\text{LOCATION\_REG } p r)v$ )  $\wedge$ 
   ( $Rg' = \text{funupd2 } Rg p r(\text{SOME } (v, \text{SOME } e))$ )  $\wedge$ 
   ( $E' = \llbracket \text{events} := E.events \cup \{e\};$ 
      $\text{intra\_causality} := E.intra\_causality \cup \{(e', e) \mid e' \in iico\};$ 
      $\text{atomicity} := E.atomicity \rrbracket$ )  $\wedge$ 

```

$$\begin{aligned}
& (X' = X \llbracket vo := X.vo \oplus (p \mapsto (\text{linear_order_extend}(X.vo\ p)\ e)) \rrbracket) \wedge \\
& (\forall e'. (e', e) \in (\text{happens_before } E' X')^+ \implies e' \in \text{viewed_events } E' p \implies (e', e) \in X.vo\ p) \\
&) \implies \\
& \text{machine_trans } P(E, M, \mathbf{F}, G, Rg, X)(\text{VIS } mvl)(E', M, \mathbf{F}, G, Rg', X') \\
&)
\end{aligned}$$

$$\text{final_state } p\ s = \exists n. (p\ n, p(n+1)) = (\text{SOME } s, \text{NONE})$$

Part XV

x86_lts_ops

lts_state = LEAF of value | LEFT of lts_state | RIGHT of lts_state | PAIR of lts_state lts_state

(eip_tracked_lts : ('s, 'a, lts_monad_visible_label)LTS → address → program_order_index → (address#program_order_index#lts_state) LTS) eip =
 { states := {(eip, po, s) | eip ∈ UNIV ∧ (po = po_initial) ∧ s ∈ lts.states};
 initial := (eip_initial, po_initial, lts.initial);
 final := {(eip, po_initial, s), x | eip ∈ UNIV ∧ (s, x) ∈ lts.final};
 trans := {(eip, po_initial, s), l, (eip', po_initial, s')} | (s, l, s') ∈ lts.trans ∧
 (∀ lmv l p v. ((l = VIS lmv) ∧ (lmv.lmv_action = ACCESS R (LOCATION_REG p REGEIP) v)) ⇒ ((eip = v) ∧ (eip' = v)) ∧
 (∀ lmv l p v. ((l = VIS lmv) ∧ (lmv.lmv_action = ACCESS W (LOCATION_REG p REGEIP) v)) ⇒ (eip' = eip)) ∧
 ((¬(∃ lmv l p d. (l = VIS lmv) ∧ (lmv.lmv_action = ACCESS d (LOCATION_REG p REGEIP) v))) ⇒ (eip' = eip))) } } }

(eip_tracked_lts_initial : address → (address#program_order_index#lts_state, unit, lts_monad_visible_label)LTS) eip =
 let s = (eip, 0, LEAF 0w) in
 { states := {s};
 initial := s;
 final := {(s, ())};
 trans := {} }

(lts_parallel : ('s1, 'a1, 'vl)LTS → ('s2, 'a2, 'vl)LTS → (('s1#s2), ('a1#a2), 'vl)LTS) lts1 lts2 =
 { states := {(s1, s2) | s1 ∈ lts1.states ∧ s2 ∈ lts2.states};
 initial := (lts1.initial, lts2.initial);
 final := {(s1, s2), (x1, x2) | (s1, x1) ∈ lts1.final ∧ (s2, x2) ∈ lts2.final};
 trans := {(s1, s2), TAU, (s1', s2')} | (s1, TAU, s1') ∈ lts1.trans ∧ s2 ∈ lts2.states } ∪
 {(s1, s2), TAU, (s1, s2')} | (s2, TAU, s2') ∈ lts2.trans ∧ s1 ∈ lts1.states } ∪
 {(s1, s2), l, (s1', s2')} | (s1, l, s1') ∈ lts1.trans ∧ (s2, l, s2') ∈ lts2.trans ∧ ¬(l = TAU) } }

(traces_of_lts : ('s, 'v, 'vl)LTS → ('s#(num → (('vl label)#s) option))set) lts =
 { (x, t) | (x = lts.initial) ∧ (∀ l' s'. (t 0 = SOME (l', s')) ⇒ (lts.initial, l', s') ∈ lts.trans) ∧
 (∀ i l' s'. (t (i + 1) = SOME (l', s')) ⇒ ∃ l s. (t i = SOME (l, s)) ∧ (s, l', s') ∈ lts.trans) } }

(completed_traces_of_lts : ('s, 'v, 'vl)LTS → ('s#(num → (('vl label)#s) option))set) lts =
 { (x, t) | (x = lts.initial) ∧
 (∀ l' s'. (t 0 = SOME (l', s')) ⇒ (lts.initial, l', s') ∈ lts.trans) ∧
 ((t 0 = NONE) ⇒ ¬(∃ l' s'. (lts.initial, l', s') ∈ lts.trans)) ∧
 (∀ i l' s'. (t (i + 1) = SOME (l', s')) ⇒ ∃ l s. (t i = SOME (l, s)) ∧ (s, l', s') ∈ lts.trans) ∧
 (∀ i l s. (t i = SOME (l, s)) ⇒ (t (i + 1) = NONE) ⇒ ¬(∃ l' s'. (s, l', s') ∈ lts.trans)) } }

(states_of_trace(trs : ('s#(num → (('vl label)#s) option))set) : 's set) =
 { s | ∃ n l tr. tr ∈ trs ∧ ((snd tr)n = SOME (l, s)) }
 ∪
 { fst tr | tr ∈ trs }

Part XVI

x86_hb_machine_thms

```
(machine_lts : proc set → state_constraint → (machine_state, unit, machine_visible_label)LTS)ps initial_state =
⟦ states :=(UNIV : machine_state set);
  initial := initial_machine_state initial_state;
  final := {};
  trans := {(s1, l, s2) | machine_trans ps s1 l s2}⟩
```

```
(machine_execution_of_event_structure E initial_state) =
let lts_prog = lts_po_of_event_structure E in
let lts_machine = machine_lts(E.procs)initial_state in
let lts = lts_parallel lts_prog lts_machine in
completed_traces_of_lts lts
```

```
final_states init_state E trs =
{st | ∃path lbl.({}, init_state), path) ∈ trs ∧
      final_state path(lbl, (E.events, st))}
```

```
hb_equivalence_thm1 =
∀E X.
well_formed_event_structure E ∧
finite E.events ∧
valid_execution E X ∧
nice_execution E X
⇒
∃M F G Rg.
(E, M, F, G, Rg, X) ∈
final_states(initial_machine_state X.initial_state)
      E
      (machine_execution_of_event_structure E X.initial_state)
```

```
partial_view_orders_well_formed E vo =
(∀p ∈ (E.procs).
  (∃es es'.
    (viewed_events E p = es ∪ es') ∧
    (∀e ∈ es'. mem_store e) ∧
    linear_order(vo p)es) ∧
  ∀e ∈ (viewed_events E p).finite{e' | (e', e) ∈ (vo p)}) ∧
(∀p. ¬(p ∈ E.procs) ⇒ (vo p = {}))
```

```
partial_valid_execution E X =
partial_view_orders_well_formed E X.vo ∧
X.write_serialization ∈ write_serialization_candidates E ∧
X.lock_serialization ∈ lock_serialization_candidates E ∧
X.rfmap ∈ reads_from_map_candidates E ∧
check_causality E X.vo(happens_before E X) ∧
check_rfmap_written E X.vo X.rfmap ∧
check_rfmap_initial E X.vo X.rfmap X.initial_state ∧
check_atomicity E X.vo
```


hb_equivalence_thm2 =
 $\forall E M \mathbf{F} G Rg X.$
finite $E.events \wedge$
 well_formed_event_structure $E \wedge$
 $(E, M, \mathbf{F}, G, Rg, X) \in$
 final_states(initial_machine_state $X.initial_state$)
 $\quad E$
 $\quad (machine_execution_of_event_structure \ E \ X.initial_state)$
 \implies
 partial_valid_execution $E \ X$

hb_machine_progress_thm =
 $\forall E mst \ es \ path \ lbl \ init.$
 $((\{\}, (initial_machine_state \ init)), path) \in$
 traces_of_lts(lts_parallel(lts_po_of_event_structure E)(machine_lts $E.procs \ init)) \wedge$
 final_state $path(lbl, (es, mst))$
 \implies
 $\exists mst'.$
 $(mst, \tau, mst') \in (machine_lts \ E.procs \ init).trans \vee$
 $(\exists es' \ l.$
 $(es, l, es') \in (lts_po_of_event_structure \ E).trans \wedge$
 $(mst, l, mst') \in (machine_lts \ E.procs \ init).trans) \vee$
 $((\forall p \ q. (\mathbf{fst}(\mathbf{snd}(\mathbf{snd} \ mst)))p \ q = [])) \wedge$
 $(\forall es' \ l. \neg((es, l, es') \in (lts_po_of_event_structure \ E).trans)))$

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