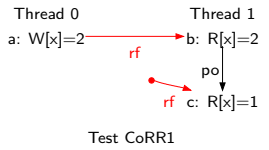
POWER and ARM Litmus Tests

http://www.cl.cam.ac.uk/~pes20/ppc-supplemental

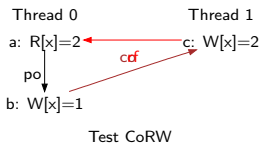
Coherence tests

CoRR1: rf,po,fr forbidden



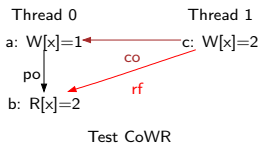
Test CoRR1

CoRW: rf,po,co forbidden



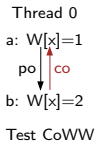
Test CoRW

CoWR: co,po,rf^{-1} forbidden



Test CoWR

CoWW: po,co forbidden

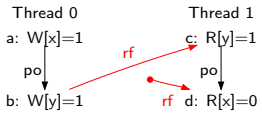


Test CoWW

4-edge 2-thread tests

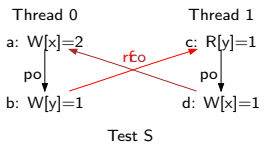
One rf

MP: rf,fr needs lwsync+RRdep



Test MP

S: rf,co needs lwsync+RWdep

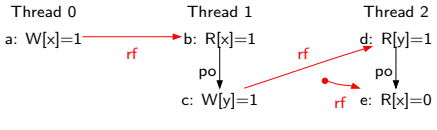


Test S

5-edge extensions along one rf edge

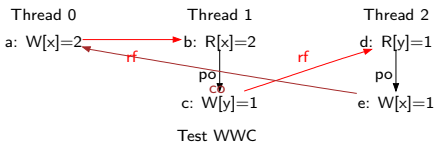
Two rf

WRC: rf,rf,fr needs lwsync+RRdep



Test WRC

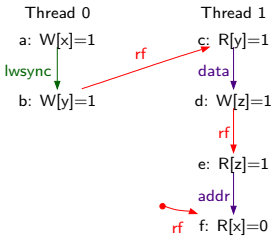
WWC: rf,rf,co needs lwsync+RWdep



Test WWC

Preserved read-read program order

PPO000–019: barrier,rf,intra-thread*,fr

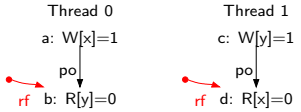


Test PPO000

6-edge extensions along two rf edges

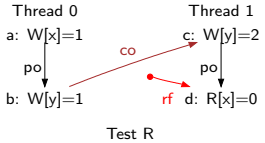
No rf

SB: fr,fr needs sync+sync



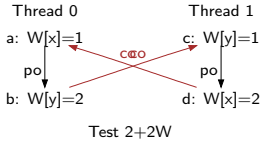
Test SB

R: co,fr needs sync+sync



Test R

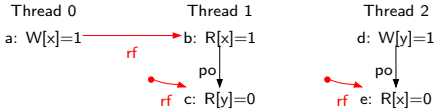
2+2W: co,co needs lwsync+lwsync



Test 2+2W

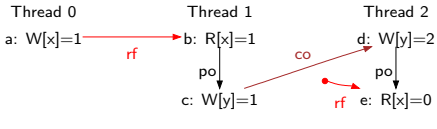
One rf

RWC: rf,fr,fr needs sync+sync



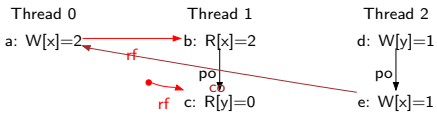
Test RWC

WRW+WR: rf,co,fr needs sync+sync



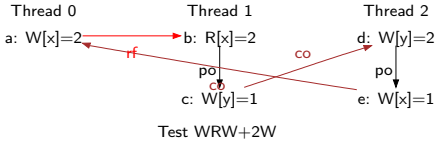
Test WRW+WR

WRR+2W: rf,fr,co needs sync+sync



Test WRR+2W

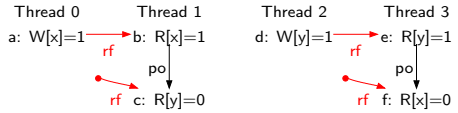
WRW+2W: rf,co,co needs lwsync+lwsync



Test WRW+2W

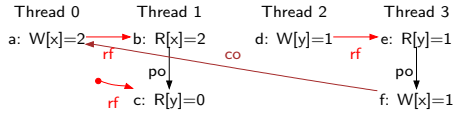
6-edge extensions along two rf edges

IRIW: rf,fr,rf,fr needs sync+sync



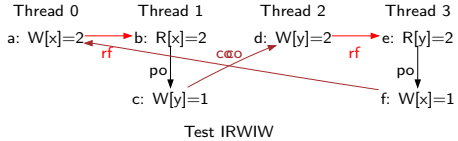
Test IRIW

IRRWIW: rf,fr,rf,co needs sync+sync



Test IRRWIW

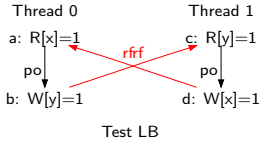
IRWIW: rf,co,rf,co needs lwsync+lwsync



Test IRWIW

Two rf

LB: rf,rf needs RWdep+RWdep



Test LB

Key

Edges:

- po program order
- rf reads-from
- co coherence order
- fr from-reads: a read from a coherence-predecessor, shown with an rf edge from the (red dot) initial state

Read-read and read-write dependencies:

RRdep ::= addr | ctrlisync

RWdep ::= addr | data | ctrl | ctrlisync

{RRdep,RWdep} < lwsync < sync

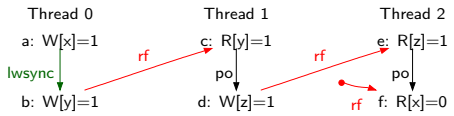
For ARM, use DMB for lwsync and sync and ctrl-ISB for ctrlisync

6-edge 3-thread tests

DRAFT – the "needs" entries need checking

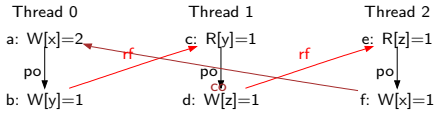
Two rf

ISA2: rf,rf,fr needs lwsync+RWdep+RRdep



Test ISA2+lwsync+po+po

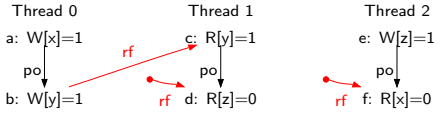
Z6.2: rf,rf,co needs lwsync+RWdep+RWdep



Test Z6.2

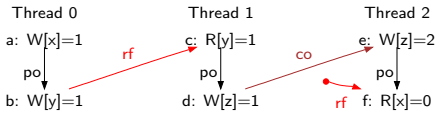
One rf

W+RWC: rf,fr,fr needs lwsync+sync+sync or sync+RWdep+sync



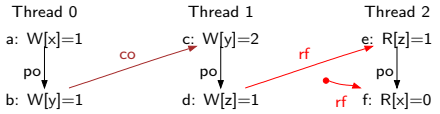
Test W+RWC

Z6.0: rf,co,fr needs lwsync+sync+sync or sync+RWdep+sync



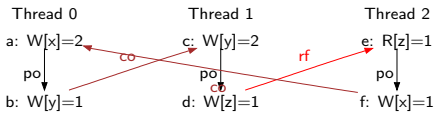
Test Z6.0

Z6.3: co,rf,fr needs sync+lwsync+sync or sync+sync+RRdep



Test Z6.3

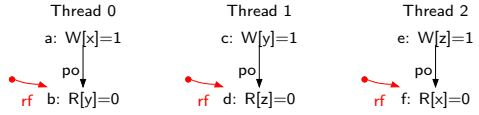
Z6.1: co,rf,co needs lwsync+lwsync+RWdep



Test Z6.1

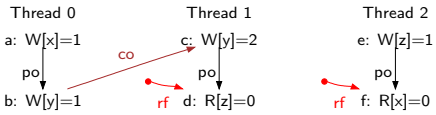
No rf

3.SB: fr,fr,fr needs sync+sync+sync



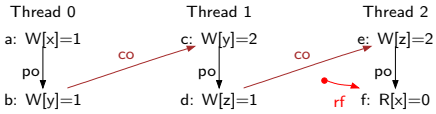
Test 3.SB

Z6.4: co,fr,fr needs sync+sync+sync



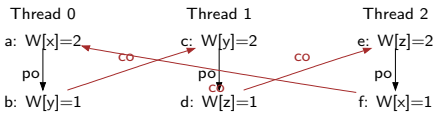
Test Z6.4

Z6.5: co,co,fr needs sync+sync+sync



Test Z6.5

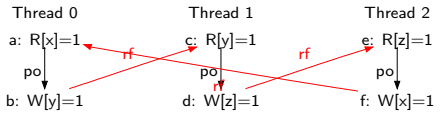
3.2W: co,co,co needs lwsync+lwsync+lwsync



Test 3.2W

Three rf

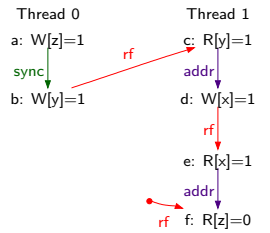
3.LB: rf,rf,rf needs RWdep+RWdep+RWdep



Test 3.LB

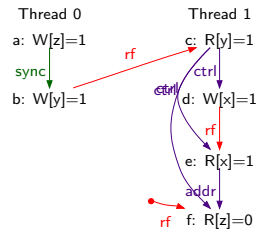
PPO variants

PPOAA: (≈ PPO000) forbidden



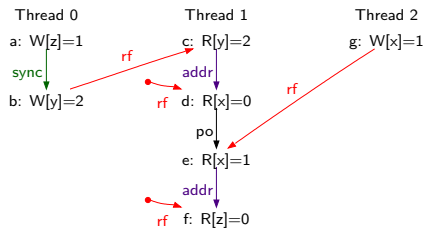
Test PPOAA

PPOCA: (≈ PPO001) allowed



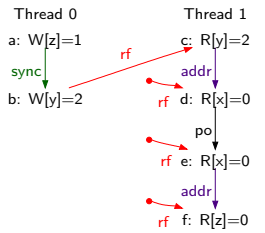
Test PPOCA

RDW: forbidden



Test RDW

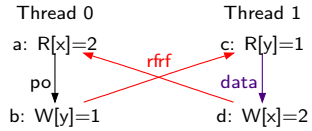
RSW: (≈ PPO002) allowed



Test RSW

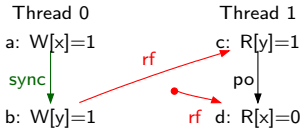
Register Shadowing

LB+rs: (register reuse on Thread 0) allowed



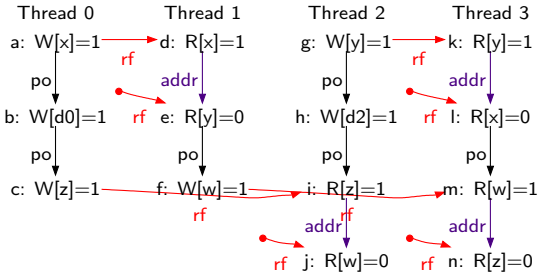
Test LB+rs

MP+sync+rs: (register reuse on Thread 1) allowed



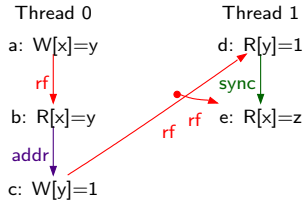
Test MP+sync+rs

IRIW+addrs-twice: allowed



Test IRIW+addrs-twice

MP+nondep+sync: allowed



Test MP+nondep+sync