Experimental Results for the Litmus Tests Cited in the Paper

(supplementary material for Mixed-size Concurrency: ARM, POWER, C/C++11, and SC)

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ARMv8 experimental results:

	Kind	Flowing	POP	HW-total	iPhone7	iPadAir2	H955-A53	OdroidC2	Nexus9	OpenQ820
01.CO-MIXED-1	—	Allow	Allow	28k/6.5G	21k/530M	3.2k/600M	0/1.2G	0/2.4G	0/600M	3.2k/1.2G
02.CO-MIXED-1b	—	Allow	Allow	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
03.CO-MIXED-2b	—	Allow	Allow	0/3.0G	—	0/600M	0/600M	0/1.2G	—	0/600M
04.CO-MIXED-2b-dmbsy	—	Allow	Allow	0/3.0G	—	0/600M	0/600M	0/1.2G	—	0/600M
05.CO-MIXED-6-sep+reader	—	Allow	Allow	0/2.4G	—	—	0/600M	0/1.2G	—	0/600M
06.CO-MIXED-6-mergedsep+reader	—	Allow	Allow	0/2.4G	—	—	0/600M	0/1.2G	—	0/600M
07.CO-MIXED-6	—	Allow	Allow	0/6.5G	0/510M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
08.CO-MIXED-20cc	—	Forbid	Forbid	1/6.5G	0/510M	0/600M	1/1.2G	0/2.4G	0/600M	0/1.2G
09.MP+misaligned2+0+addr	—	Forbid	Forbid	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
10.MP+misaligned2+1+addr	—	Allow	Allow	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
11.MP+misaligned2+3+addr	—	Allow	Allow	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
12.MP+misaligned2+7+addr	—	Allow	Allow	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
13.MP+misaligned2+15+addr	—	Allow	Allow	283/6.5G	0/530M	0/600M	70/1.2G	213/2.4G	0/600M	0/1.2G
14.MP+misaligned2+31+addr	—	Allow	Allow	215/6.5G	0/530M	0/600M	59/1.2G	156/2.4G	0/600M	0/1.2G
15.MP+misaligned2+63+addr	—	Allow	Allow	20M/6.5G	3.5k/530M	0/600M	6.8M/1.2G	13M/2.4G	0/600M	1.2k/1.2G
16.MP+misaligned2+127+addr	—	Allow	Allow	35k/6.5G	808/530M	0/600M	3.6k/1.2G	1.9k/2.4G	0/600M	29k/1.2G
17.MP+misaligned2+255+addr	—	Allow	Allow	37k/4.1G	963/530M	0/600M	2.3k/1.2G	—	0/600M	33k/1.2G
18.MP+misaligned2+511+addr	—	Allow	Allow	16k/4.1G	1.7k/530M	0/600M	545/1.2G	—	0/600M	14k/1.2G
19.MP+misaligned2+0x+addr	—	Forbid	Forbid	0/4.1G	0/530M	0/600M	0/1.2G	—	0/600M	0/1.2G
20.MP+misaligned2+1x+addr	—	Allow	Allow	0/4.1G	0/530M	0/600M	0/1.2G	—	0/600M	0/1.2G
21.MP+misaligned2+3x+addr	—	Allow	Allow	0/4.1G	0/530M	0/600M	0/1.2G	—	0/600M	0/1.2G
22.MP+misaligned2+7x+addr	—	Allow	Allow	0/4.1G	0/530M	0/600M	0/1.2G	—	0/600M	0/1.2G
23.MP+misaligned2+15x+addr	—	Allow	Allow	469k/4.1G	0/530M	0/600M	469k/1.2G	—	0/600M	0/1.2G
24.MP+misaligned2+31x+addr	—	Allow	Allow	393k/4.1G	0/530M	0/600M	393k/1.2G	—	0/600M	0/1.2G
25.MP+misaligned2+63x+addr	—	Allow	Allow	76M/4.1G	11M/530M	5.5M/600M	8.3M/1.2G	—	2.1k/600M	51M/1.2G
26.MP+misaligned2+127x+addr	—	Allow	Allow	19M/4.1G	4.0M/530M	3.1M/600M	9.1k/1.2G	—	2.8k/600M	12M/1.2G
27.MP+misaligned2+255x+addr	—	Allow	Allow	33M/4.1G	3.6M/530M	5.5M/600M	8.0k/1.2G	—	4.0k/600M	24M/1.2G
28.MP+misaligned2+511x+addr	—	Allow	Allow	46M/4.1G	2.5M/530M	7.6M/600M	4.4k/1.2G	—	5.5k/600M	36M/1.2G
29.MP+dmbsy+misaligned2+0	—	Forbid	Forbid	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
30.MP+dmbsy+misaligned2+1	—	Allow	Allow	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
31.MP+dmbsy+misaligned2+3	—	Allow	Allow	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
32.MP+dmbsy+misaligned2+7	—	Allow	Allow	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
33.MP+dmbsy+misaligned2+15	—	Allow	Allow	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
34.MP+dmbsy+misaligned2+31	—	Allow	Allow	0/6.5G	0/530M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
35.MP+dmbsy+misaligned2+63	—	Allow	Allow	1.9M/6.5G	30/530M	1/600M	782k/1.2G	1.1M/2.4G	0/600M	0/1.2G
36.MP+dmbsy+misaligned2+127	—	Allow	Allow	2.8k/6.5G	33/530M	45/600M	1.4k/1.2G	1.1k/2.4G	0/600M	196/1.2G
37.MP+dmbsy+misaligned2+255	—	Allow	Allow	1.6k/4.1G	32/530M	13/600M	1.4k/1.2G	—	0/600M	143/1.2G
38.MP+dmbsy+misaligned2+511	—	Allow	Allow	455/4.1G	38/530M	1/600M	244/1.2G	—	0/600M	172/1.2G
39.MP+dmbsy+misaligned2+0x	—	Forbid	Forbid	0/4.1G	0/530M	0/600M	0/1.2G	—	0/600M	0/1.2G
40.MP+dmbsy+misaligned2+1x	—	Allow	Allow	0/4.1G	0/530M	0/600M	0/1.2G	—	0/600M	0/1.2G
41.MP+dmbsy+misaligned2+3x	—	Allow	Allow	0/4.1G	0/530M	0/600M	0/1.2G	—	0/600M	0/1.2G
42.MP+dmbsy+misaligned2+7x	—	Allow	Allow	0/4.1G	0/520M	0/600M	0/1.2G	—	0/600M	0/1.2G
43.MP+dmbsy+misaligned2+15x	—	Allow	Allow	0/4.1G	0/520M	0/600M	0/1.2G	—	0/600M	0/1.2G
44.MP+dmbsy+misaligned2+31x	—	Allow	Allow	0/4.1G	0/520M	0/600M	0/1.2G	—	0/600M	0/1.2G
45.MP+dmbsy+misaligned2+63x	—	Allow	Allow	1/4.1G	1/510M	0/600M	0/1.2G	—	0/600M	0/1.2G
46.MP+dmbsy+misaligned2+127x	—	Allow	Allow	181/4.1G	0/510M	0/600M	0/1.2G	—	0/600M	181/1.2G
47.MP+dmbsy+misaligned2+255x	—	Allow	Allow	120/4.1G	0/510M	0/600M	0/1.2G	—	0/600M	120/1.2G
48.MP+dmbsy+misaligned2+511x	—	Allow	Allow	85/4.1G	0/510M	0/600M	0/1.2G	—	0/600M	85/1.2G
49.MP+stp+addr+60	—	Allow	Allow	20M/6.5G	1.6k/510M	0/600M	6.6M/1.2G	13M/2.4G	0/600M	318/1.2G
50.MP+str+ldp	—	Allow	Allow	0/6.5G	0/510M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
51.MP+dmbsy+ldp-addr+BIS3	—	Forbid	Forbid	0/6.5G	0/510M	0/600M	0/1.2G	0/2.4G	0/600M	0/1.2G
52.PPOCA-MIXED-1	—	Allow	Allow	34k/6.5G	5.9k/510M	1.0k/600M	27k/1.2G	0/2.4G	0/600M	0/1.2G
53.PPOCA-MIXED-2	—	Allow	Allow	76k/6.5G	13k/510M	17k/600M	46k/1.2G	0/2.4G	0/600M	0/1.2G
54.PPOCA-MIXED-3	—	Allow	Allow	86k/6.5G	18k/510M	32k/600M	37k/1.2G	0/2.4G	0/600M	41/1.2G
55.IRIW-MIXED-1	—	Allow	Allow	0/2.4G	—	—	0/600M	0/1.2G	—	0/600M

The `MP+misaligned2+NNNx+addr` variants of the `MP+misaligned2+NNN+addr` tests do the reads on Thread 1 in the opposite order, as do the `MP+dmbsy/lwsync+misaligned2+NNNx` variants of the `MP+dmbsy/lwsync+misaligned2+NNN` tests.

- Flowing, Pop: our models. These match the architectural intent for all except the §2.7 `MP+dmbsy+ldp-addr+BIS3`.
- HW-total: sum of the following observed hardware results
- iPadAir2: Apple A8X SoC/CPU, three-core
- H955-A53: LG H955 phone, Qualcomm Snapdragon810 SoC, ARM Cortex-A57/A53 CPU, quad+quad core (using the A53 cores)
- OdroidC2: ODROID-C2 development board, Amlogic S905 SoC, ARM Cortex-A53 CPU, quad-core
- Nexus9: Google Nexus 9 tablet, Nvidia Tegra K1 SoC, Nvidia Denver CPU, dual-core
- OpenQ820: Open-Q 820 development kit, Qualcomm Snapdragon 820 SoC, Qualcomm Krait CPU, 4-core

POWER 7 Experimental results:

	Kind	Model	POWER7
01.CO-MIXED-1	—	Allow	500k/3.5G
02.CO-MIXED-1b	—	Allow	0/3.5G
03.CO-MIXED-2b	—	Allow	603/2.2G
04.CO-MIXED-2b-sync	—	Allow	48k/2.2G
05.CO-MIXED-6-sep+reader	—	Allow	7.3k/1.8G
06.CO-MIXED-6-mergedsep+reader	—	Allow	6.8k/1.8G
07.CO-MIXED-6	—	Allow	0/3.5G
08.CO-MIXED-20cc	—	Allow	0/3.4G
09.MP+misaligned2+0+addr	—	Forbid	0/3.5G
10.MP+misaligned2+1+addr	—	Allow	0/3.4G
11.MP+misaligned2+3+addr	—	Allow	0/3.4G
12.MP+misaligned2+7+addr	—	Allow	0/3.4G
13.MP+misaligned2+15+addr	—	Allow	0/3.4G
14.MP+misaligned2+31+addr	—	Allow	0/3.4G
15.MP+misaligned2+63+addr	—	Allow	0/3.4G
16.MP+misaligned2+127+addr	—	Allow	8.1M/3.4G
17.MP+misaligned2+255+addr	—	Allow	3.9M/6.6G
18.MP+misaligned2+511+addr	—	Allow	2.9M/6.4G
19.MP+misaligned2+0x+addr	—	Forbid	0/6.4G
20.MP+misaligned2+1x+addr	—	Allow	0/6.4G
21.MP+misaligned2+3x+addr	—	Allow	0/6.4G
22.MP+misaligned2+7x+addr	—	Allow	0/6.4G
23.MP+misaligned2+15x+addr	—	Allow	0/6.4G
24.MP+misaligned2+31x+addr	—	Allow	4.7M/6.4G
25.MP+misaligned2+63x+addr	—	Allow	4.0M/6.4G
26.MP+misaligned2+127x+addr	—	Allow	4.3M/6.4G
27.MP+misaligned2+255x+addr	—	Allow	4.1M/6.4G
28.MP+misaligned2+511x+addr	—	Allow	8.9M/6.4G
29.MP+lwsync+misaligned2+0	—	Forbid	0/3.5G
30.MP+lwsync+misaligned2+1	—	Allow	0/3.5G
31.MP+lwsync+misaligned2+3	—	Allow	0/3.5G
32.MP+lwsync+misaligned2+7	—	Allow	0/3.5G
33.MP+lwsync+misaligned2+15	—	Allow	0/3.5G
34.MP+lwsync+misaligned2+31	—	Allow	0/3.5G
35.MP+lwsync+misaligned2+63	—	Allow	22k/3.5G
36.MP+lwsync+misaligned2+127	—	Allow	337k/3.4G
37.MP+lwsync+misaligned2+255	—	Allow	97k/6.6G
38.MP+lwsync+misaligned2+511	—	Allow	350k/6.6G
39.MP+lwsync+misaligned2+0x	—	Forbid	0/6.6G
40.MP+lwsync+misaligned2+1x	—	Allow	0/6.6G
41.MP+lwsync+misaligned2+3x	—	Allow	0/6.6G
42.MP+lwsync+misaligned2+7x	—	Allow	0/6.6G
43.MP+lwsync+misaligned2+15x	—	Allow	0/6.6G
44.MP+lwsync+misaligned2+31x	—	Allow	26k/6.6G
45.MP+lwsync+misaligned2+63x	—	Allow	25k/6.6G
46.MP+lwsync+misaligned2+127x	—	Allow	3.6M/6.6G
47.MP+lwsync+misaligned2+255x	—	Allow	4.3M/6.6G
48.MP+lwsync+misaligned2+511x	—	Allow	5.0M/6.6G
49.MP+stmw+addr+124	—	Allow	8.7M/3.4G
50.MP+std+lmw	—	Allow	12M/3.4G
51.MP+lwsync+lmw-addr+BIS3	—	Forbid	4.7k/3.5G
52.PPOCA-MIXED-1	—	Allow	0/3.4G
53.PPOCA-MIXED-2	—	Allow	0/3.4G
54.PPOCA-MIXED-3	—	Allow	7/3.4G
55.IRIW-MIXED-1	—	Allow	46k/1.8G
56.SCA-1	—	Forbid	0/2.1G

- Model: our model. This matches the architectural intent for all except the §2.7 `MP+lwsync+lmw-addr+BIS3`.
- POWER7: IBM POWER 730 server, POWER 7 CPU, 48 hardware threads