SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

The model R-1250 is a wide range superheterodyne surveillance receiver that is continuously tunable, covering the range of 100Hz to 1GHz in 8 bands. The receiver detects RF signals in the form of continuous wave (CW) or modulated carriers, both amplitude (AM) and frequency modulated (FM).

The simplified block diagram of figure 4-1 shows the use of three conversion sections that divide the input range into specific frequency bands. The conversion sections contain the preselection filters and the mixer circuits used to heterodyne the tuned input signal to an intermediate frequency. Two intermediate frequencies are used to provide a full range of selectable bandwidths. The output from the selected IF section is routed to the appropriate detector/discriminator which provides the audio and video output signal.

The receiver utilizes precision phase locked loop synthesizer circuits to create the required local oscillator signals, thus providing accurate frequency control and high resolution.

Digital circuits within the receiver provide timing and control of the various functions and displays that originate from front panel switch selection or the automatic control function provided by the IEEE-488 General Purpose Interface Bus.

Direct current operating voltages used by the various circuits are derived from the power section of the receiver which converts the input power into eight individually regulated DC voltages.

4.2 FUNCTIONAL DESCRIPTION

The block diagram in figure 4-2 is detailed to show the heterodyne stages and the local oscillator (LO) values used to derive the two intermediate frequencies. The conversion stages cover the tuning range of the receiver in eight individual bands as shown in table 4-1. Input signals to the receiver are applied to a programmable step attenuator and then routed to the appropriate conversion stage by automatic band selection relays. The RF section is used for converting the frequencies within bands 3 through 8. This section used three individual heterodyne stages to produce two separate output frequencies.

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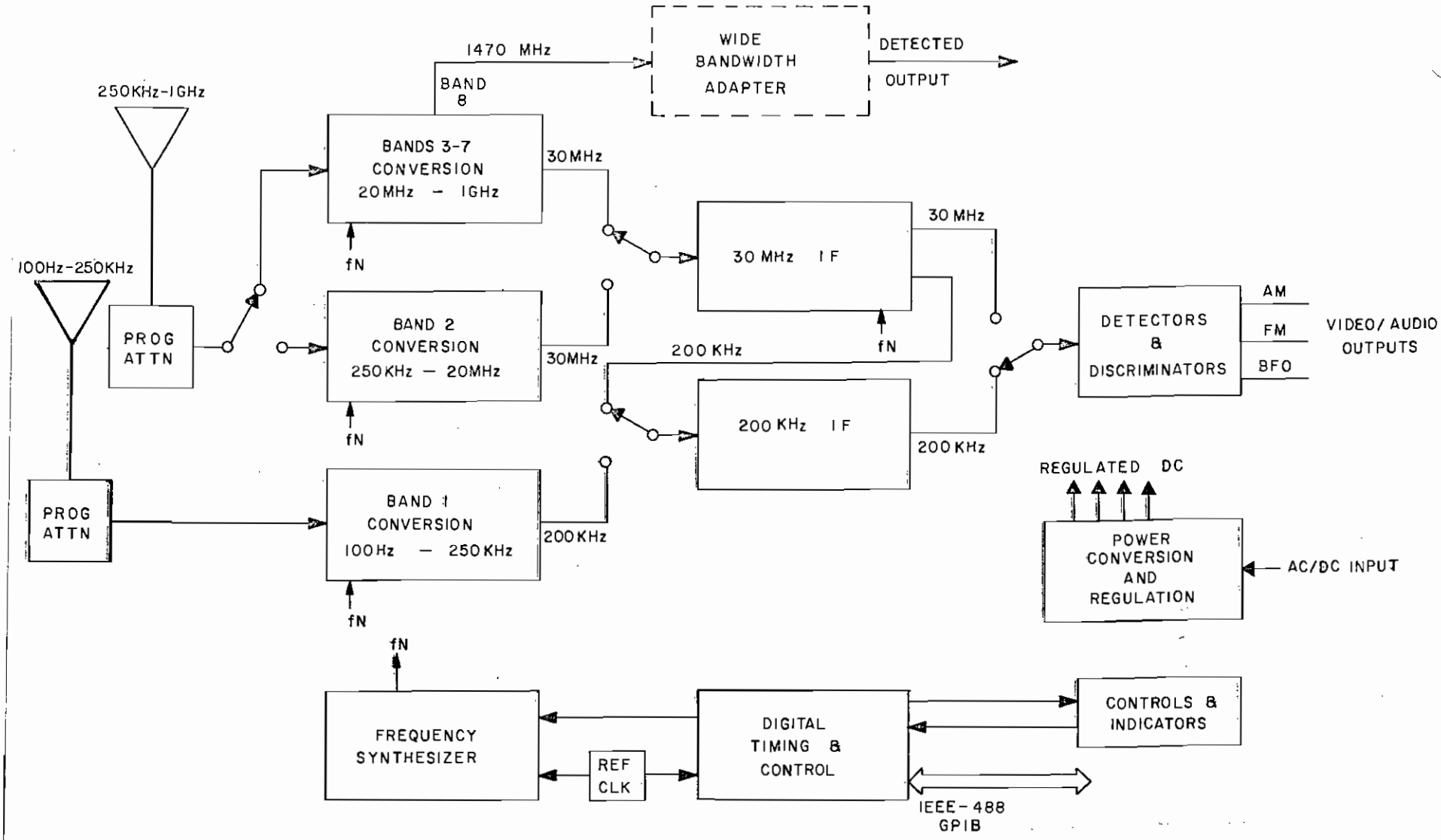

FIGURE 4-1 SIMPLIFIED BLOCK DIAGRAM

TABLE 4-1

FREQUENCY BANDS

BAND 1	100 Hz to 250 KHz	BAND 5	350 MHz to 550 MHz
BAND 2	250 KHz to 20 MHz	BAND 6	550 MHz to 750 MHz
BAND 3	20 MHz to 200 MHz	BAND 7	750 MHz to 1 GHz
BAND 4	200 MHz to 350 MHz	BAND 8	20 MHz to 1 GHz

NOTE: Band 8 is only used when the Wide Bandwidth Adapter is integrated with the receiver.

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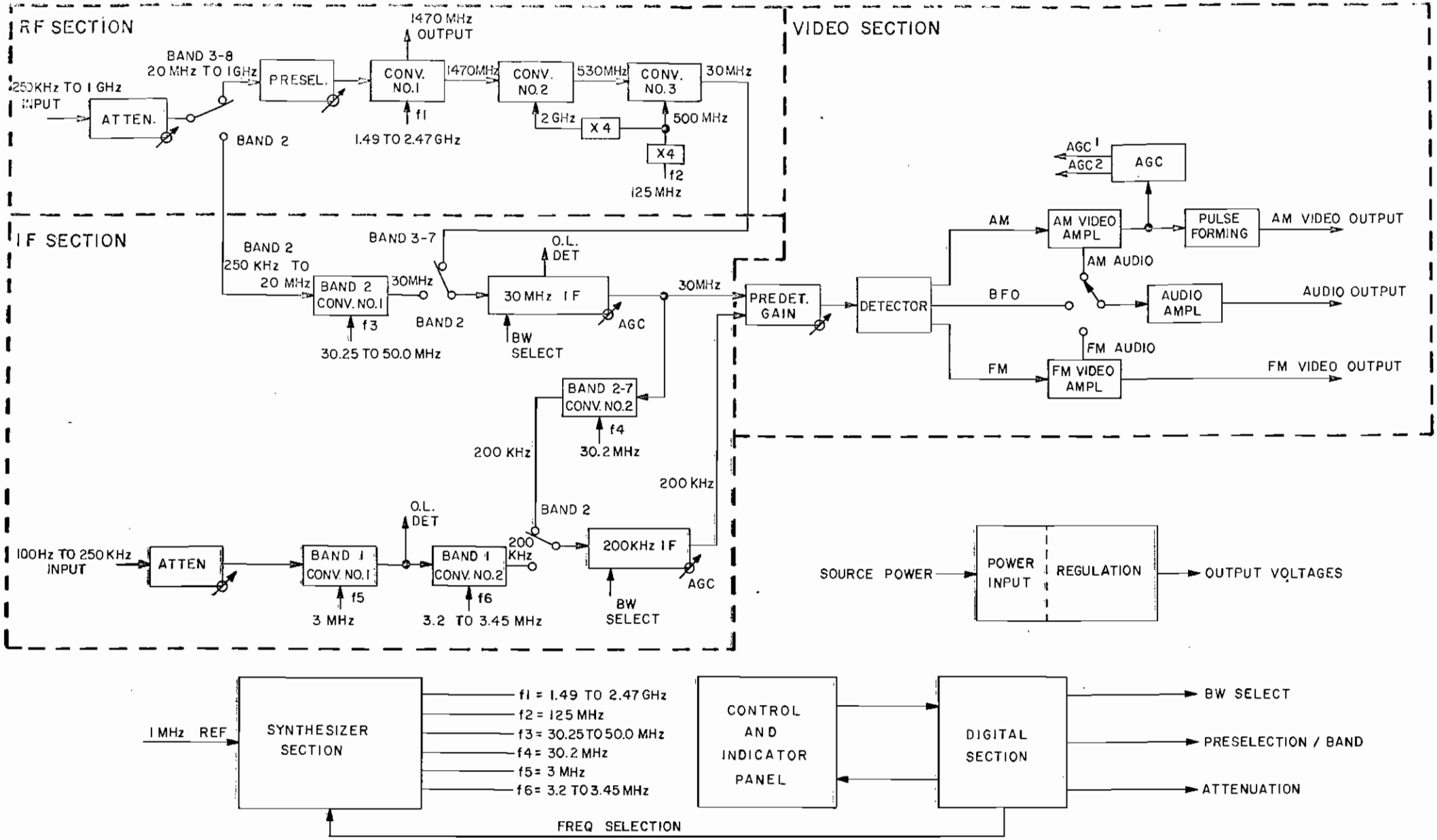

FIGURE 4-2 SIGNAL CONVERSION DIAGRAM
4-7/4-8

4.2 FUNTIONAL DESCRIPTION(continued)

The first conversion stage produces a difference frequency of 1470 MHz. This first conversion product is directed by relay to either the rear panel connector of the receiver for interfacing the optional Wide Bandwidth Adapter, or the signal is routed through two consecutive mixer stages to produce the receivers 30 MHz intermediate frequency.

The IF section shown in the block diagram includes conversion stages for signals within band 2 as well as band 1. The range of frequencies within band 2, 250 KHz to 20 MHz, are converted to a 30 MHz intermediate frequency by the first mixer stage and routed to the 30 MHz IF Strip for further processing. Note that the IF section includes a second converter for band 2-7 frequencies as part of the output from the IF Strip. The second converter mixes the 30 MHz IF output with a fixed LO frequency of 30.2 MHz to produce a difference of 200 KHz. This converted signal becomes the input to the 200KHz IF and is used when a bandwidth less than 5 0 KHz has been selected for frequencies within bands 2 through 7.

Frequencies within the range of band 1, 100 Hz to 250 KHz, are converted to a 200 KHz intermediate frequency using two mixer stages. The first mixer is an up-converter that produces the sum of two signals, the band 1 received frequency and a 3 MHz LO signal. The first mixer stage output, which is always 3 MHz above the band 1 frequency, is routed to a second converter where it is mixed with a variable LO frequency ranging from 3.2 to 3.45 MHz to produce a fixed 200 KHz intermediate frequency.

4.3 RF SECTION

The RF section of the receiver is shown in the diagram of figure 4-3. The RF conversion circuitry is contained on two microwave assemblies, M1 and M2. The microwave assemblies also contain portions of the synthesizer circuitry, as indicated by the shaded areas of the diagram.

Input signals are applied through a transfer relay that permits the selection of an alternate input comparison signal used for calibrating the unit. The input (or calibration) signal is routed to a programmable attenuator that is variable in 10dB steps from 0 to 100dB, providing an output that is directed by the band selection relays to the appropriate conversion section. The RF section provides the conversion stages for frequencies within bands 3 through 8. Frequencies within these bands are applied through coaxial switch contacts to the appropriate discrete filter networks that form the preselector. The filter networks are selected as a function of the tuned frequency and improve the receivers performance by rejecting any signal outside the passband. Band 3 frequencies are routed through a low pass filter network while bands 4 through 7 are band - pass filtered frequencies within band 8, which continuously covers the frequencies of bands 3 through 7, are filtered by a low pass network.

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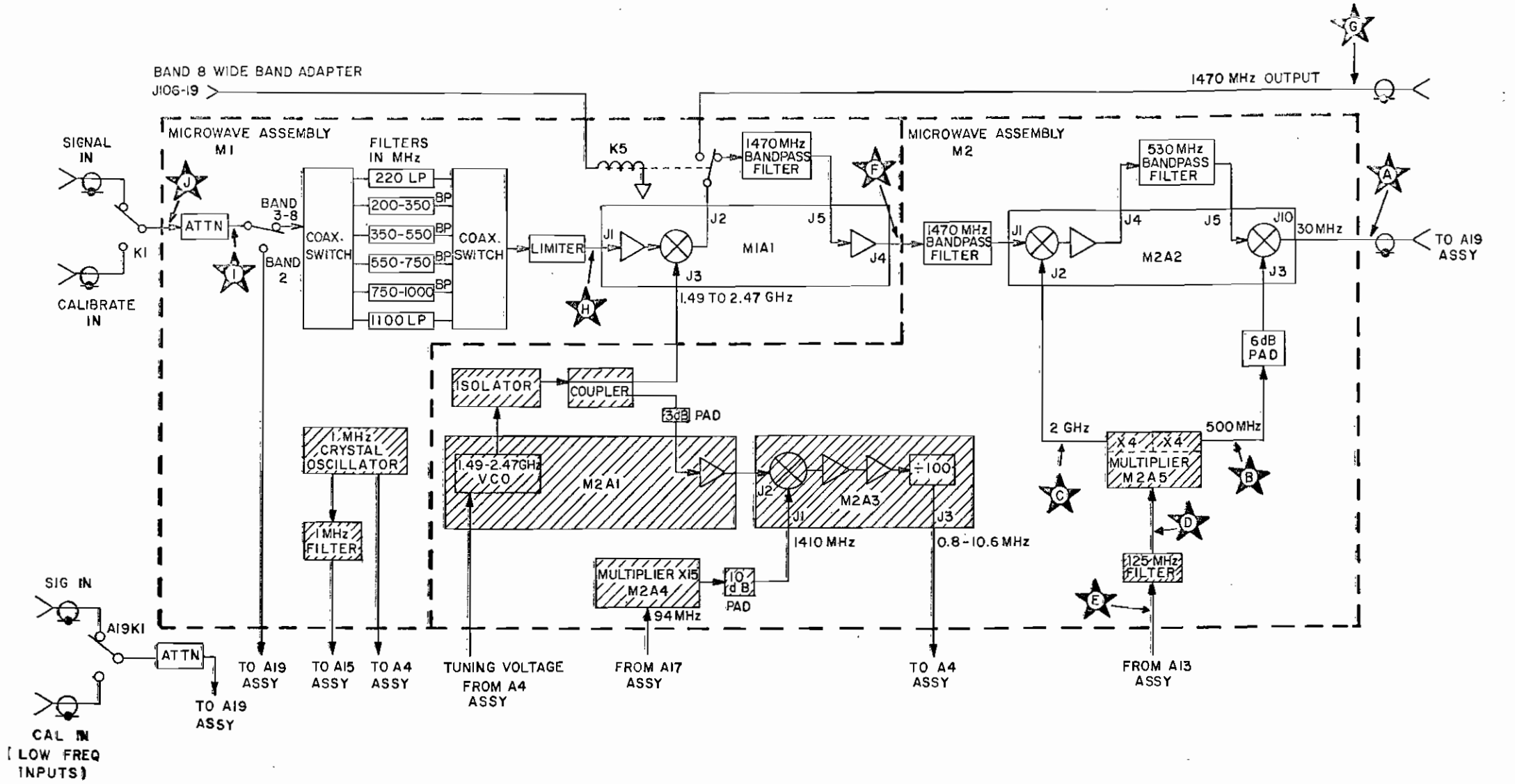

FIGURE 4-3 RF SECTION SIGNAL FLOW DIAGRAM
4-11/4-12

4.3 RF SECTION (continued)

The preselector output is applied to a wide band limiter for protection against transient spikes, before going through an amplifier that has a wide dynamic range and a low noise figure. The amplified signal is routed to the first conversion stage where the tuned input signal is heterodyned with a LO signal to produce an output of 1470 MHz. The LO signal is derived from a VCO that generates a frequency covering the range of 1490 to 2470 MHz. When the wide bandwidth adapter is used with the receiver, a band 8 selected signal energizes the relay K5, which routes the 1470 MHz signal to an external connector for interfacing the adapter. For preselected frequencies within bands 3 through 7, the 1470 MHz signal is routed through bandpass filters and an amplifier stage to a second converter. The 1470 MHz input is mixed with a fixed LO frequency of 2 GHz to produce an output frequency of 530 MHz. This signal is amplified and filtered before going into a third conversion stage where it is mixed with a fixed LO frequency of 500 MHz, to derive the 30 MHz intermediate frequency.

4.4 IF SECTION

The receivers wide range of input frequencies are separated into the individual bands shown in table 4-1. The frequencies within each band are heterodyned into intermediate frequencies and processed by the IF amplifier stages. The range of frequencies within bands 3 through 7 are converted to 30 MHz signal by the circuits within the RF section of the receiver. The range of frequencies within bands 1 and 2 use individual conversion stages that are part of the IF section.

The conversion and amplification stages for both intermediate frequencies are shown in figure 4-4. Two intermediate frequencies and the use of multiple bandwidth filters ensures maximum sensitivity and signal selectivity over the full range of the receiver. The upper half of the diagram shows the conversion stages for band 2 frequencies that range from 250 KHz to 20 MHz followed by the amplification stages for the 30 MHz, intermediate frequency. The lower half of the diagram shows the conversion and amplification stages of the 200 KHz IF which process band 1 frequencies ranging from 100Hz to 250 KHz.

The frequencies within band 2 are routed for conversion from the band selection relay to a 20 MHz low pass filter and applied to a low noise amplifier that has a wide dynamic range. The signal is then applied to a double balanced mixer where it is heterodyned with an LO frequency ranging from 30.25 to 50 MHz. The difference frequency of 30 MHz is amplified and filtered before being routed through another relay to the 30 MHz IF amplification strip. The input to the 30 MHz IF strip is thus relay selected from either the conversion stage for band 2 frequencies or the RF section which provides conversion of frequencies within band 3 through 7.

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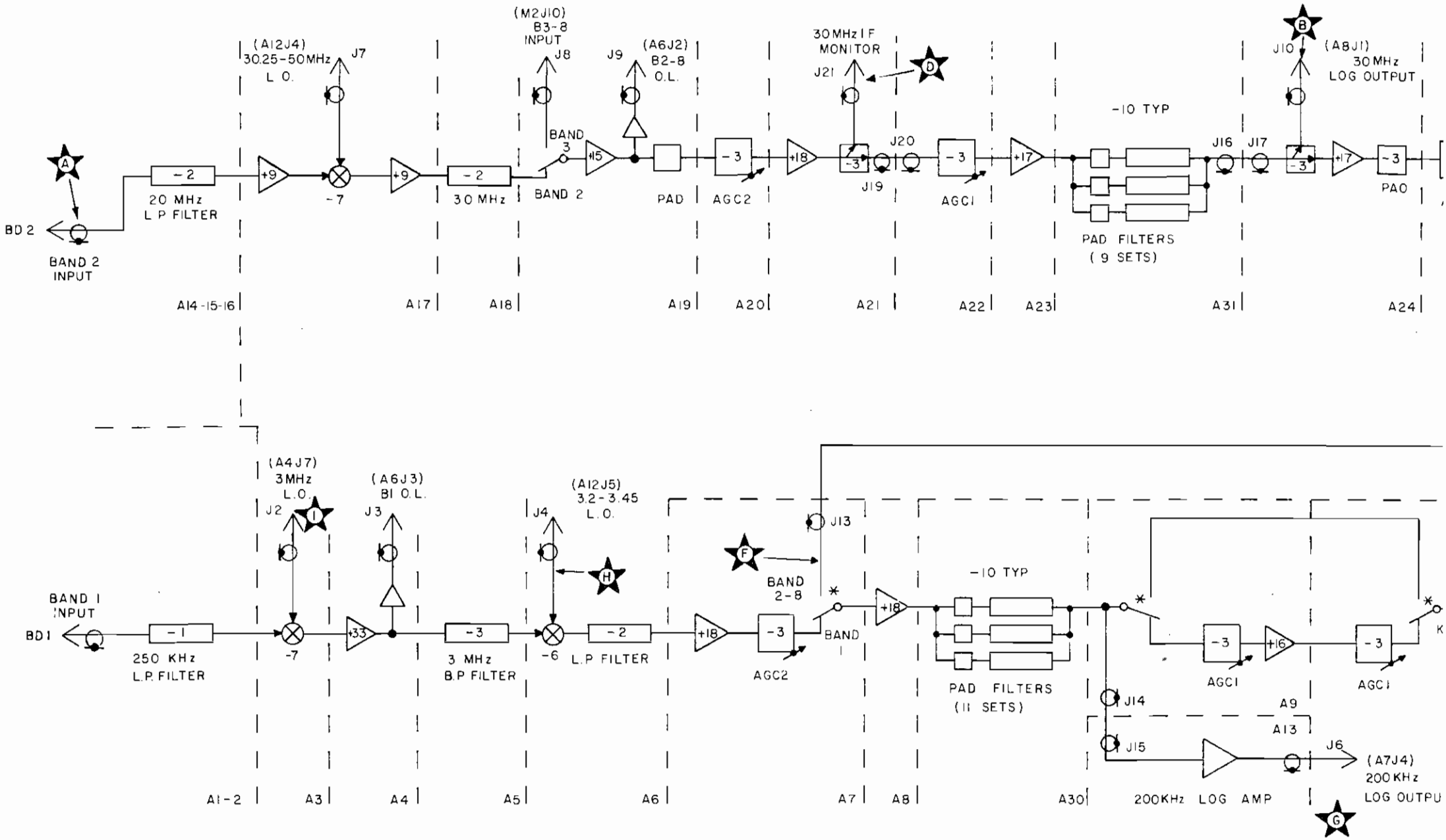
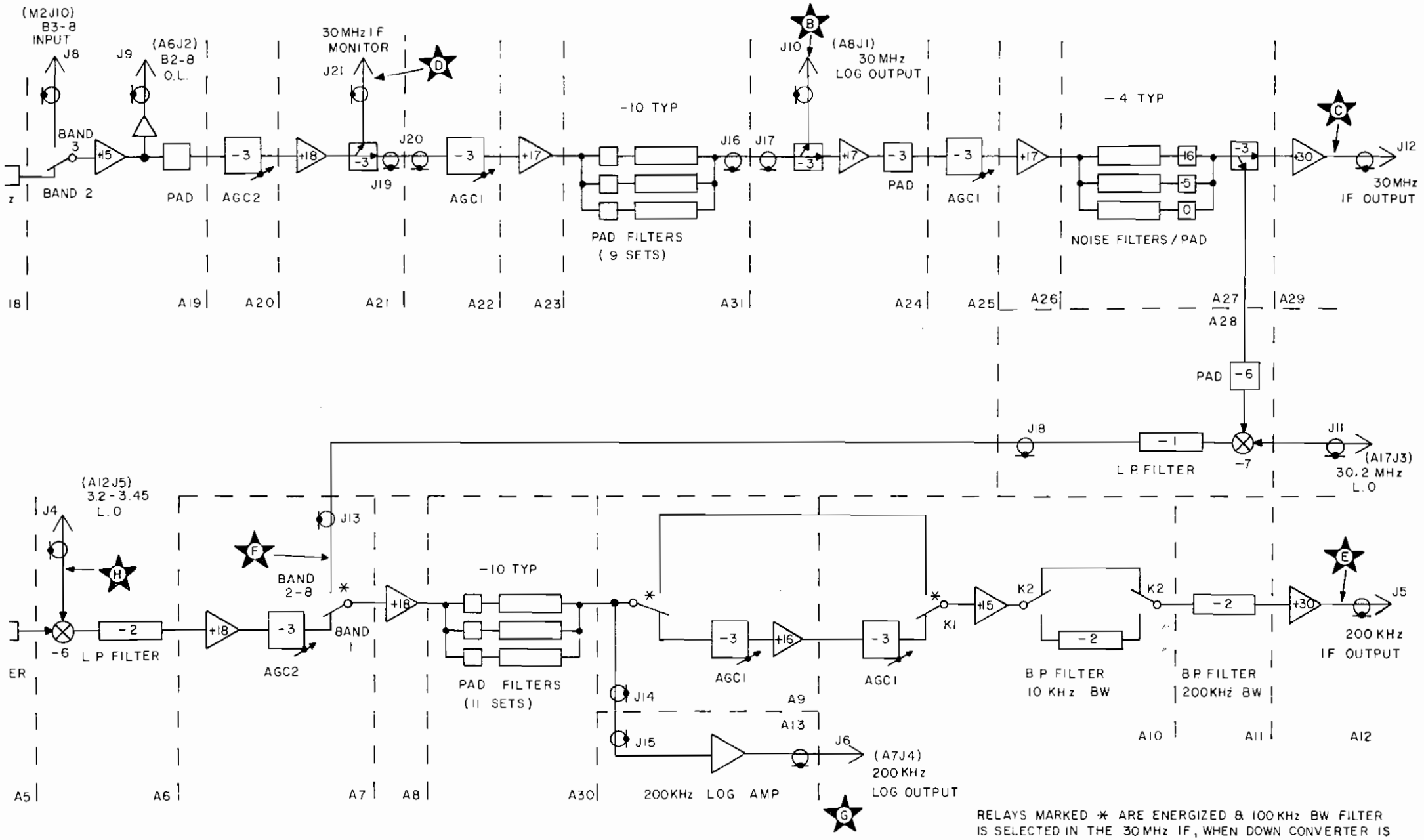

(M2J10)
B3-8
INPUT
(A12J4)
30.25-50MHz
L O.
J7
J8
J9
(A6J2)
B2-8
O.L.
30MHz I F
MONITOR
J21
D
J10
B
(A8J1)
30MHz
LOG OUTPUT
-10 TYP
A
BAND
3
+15
-2
+9
+9
-2
-3
+18
-3
+18
-3
-3
+17
-3
+17
-3
J20
J19
J16
J17
BD 2
BAND 2
INPUT
20 MHz
L P FILTER
-7
30 MHz
BAND 2
PAD
AGC2
AGC1
PAD FILTERS
(9 SETS)
PAO
A14-15-16
A17
A18
A19
A20
A21
A22
A23
A31
A24
(A4J7)
3MHz
L.O.
J2
I
(A6J3)
BI O.L.
J3
(A12J5)
3.2-3.45
L.O.
J4
H
F
J13
BAND
2-8
BAND I
INPUT
BD1
-1
250 KHz
L.P. FILTER
-7
+33
-3
3 MHz
B.P FILTER
-6
-2
L.P FILTER
+18
-3
AGC2
BAND
I
+18
-10 TYP
PAD FILTERS
(11 SETS)
-3
AGC1
+16
-3
AGC1
K
J14
A9
A13
J15
J6
(A7J4)
200KHz
LOG OUTPU
A1-2
A3
A4
A5
A6
A7
A8
A30
200KHz LOG AMP
G



RELAYS MARKED * ARE ENERGIZED & 100KHz BW FILTER IS SELECTED IN THE 30MHz IF, WHEN DOWN CONVERTER IS ENABLED. A10K2 IS ENERGIZED FOR BW OF 2KHz OR LESS.

FIGURE 4-4 IF SECTION SIGNAL FLOW DIAGRAM
4-15/4-16

4.4 IF SECTION (continued)

The relay selected input signal is first amplified and the output is monitored for detection RF overload conditions. To prevent overloading of the broader front-end stages by strong signals outside of the IF passband, an overload detection circuit is provided. The circuit functions by monitoring the signal and routing it through peak detection and threshold comparison stages. The detected signal is compared with a DC voltage to provide a drive signal when an overload condition exists. The drive signal activates a light emitting diode on the receiver front panel in the manual mode and automatically controls the input attenuator when in the auto mode.

The amplifier output is sent through an AGC stage, amplified again and routed through a power splitter. Automatic gain control is accomplished using voltage controlled pin diode attenuators for AGC 1 and AGC 2 stages. The AGC stages use control signals that vary the pin diode attenuator of each stage to optimize the sensitivity and dynamic range.

The power splitter provides a signal path to rear panel connector used to monitor the 30 MHz IF, and also couples the signal to the nine sets of selectable attenuator/filter networks used to establish the IF bandwidth. Each bandpass filter is preceded by an equalization network that compensates for insertion loss. The selectable bandwidth filters follow a 1,2,5 sequence, starting at 50 KHz and ending at 20 MHz. The output from the selected bandwidth filter is routed through another splitter to a sequential log detector in the video section, and is also amplified and coupled to selectable noise filter networks, The filters are selected as a function of the bandwidth, and minimize the noise generated by the preceding high gain amplifier stages.

A third power splitter follows the noise filters and routes half of the signal through an amplifier stage for coupling to the video detectors. The remaining output from the splitter is applied to a double balanced mixer and is heterodyned with a fixed LO frequency to produce a 200 KHz output. The converted signal is filtered and routed to a band selection relay for use when bandwidths less than 50 KHz have been selected for receiver input signals within bands 2 through 7 (250 KHz to 1000MHz).

Received frequencies within the range of 100 Hz to 250 KHz are routed from the attenuator to the band 1 frequency conversion stages. The signal is applied to a 250 KHz low pass filter and coupled to a double balanced mixer where it is up-coverted by mixing with a fixed 3 MHz LO. The sum of the two frequencies is amplified and the signal is monitored for detecting a signal overload. The amplified signal is routed through a bandpass filter into a second converter for mixing with a variable LO frequency that ranges from 3.2 to 3.45 MHz. The difference frequency of the signals is 200 KHz, which is amplified and routed to a band selection relay. The 200 KHz input to the next amplifier stage is selected from either the converted frequency of band 1, or the signal derived from the 30 MHz IF that has been converted from signals within the range of bands 2 through 7.

The amplified 200 KHz intermediate frequency is routed through one of eleven selectable bandwidth filters that follow the same 1,2,5 sequence of the filter networks in the 30 MHz IF. Each filter is preceded by a loss equalization network and range in bandwidth from 50 Hz up to 100 KHz. The output from the selected bandwidth filter is routed through an amplifier that provides a logarithmic output, and is also routed through two stages of gain control followed by amplifier and filter stages that couple the 200 KHz IF signal to the video section.

The two stages of automatic gain control are automatically bypassed when the band selection relay derives the input signal from the 30 MHz IF. When an IF bandwidth of 2 KHz or less is selected, relay K2 is energized and routes the IF signal through an additional bandpass filter that reduces broadband noise before being routed to the video section.

4.5 VIDEO SECTION

The block diagram in figure 4-5 shows the printed circuit card assemblies that are used in the video section of the receiver. The input signal to the video circuits is automatically selected by the IF Transfer relay from either the 30 MHz or the 200 KHz IF output, depending on the band and bandwidth combination used. The signal is applied to a predetection gain stage that has selectable step attenuators in addition to a variable predetection gain control. The output signal from the predetection gain stage is routed to the relay selected amplifier before going to the detectors.

Linear IF signals from the predetection amplifiers are routed to the corresponding 200 KHz or 30 MHz, AM and FM detectors. Logarithmic inputs from the 200 KHz and the 30 MHz IF, are switch selectable depending on the position of the front panel log/linear switch.

BFO circuits that aid the detection of continuous wave (CW) signals are provided for both the 200 KHz and the 30 MHz IF. The beat frequency for the 200 KHz detector is variable within ±1KH by a front panel BFO control. The BFO signal for the 30 MHz IF is derived from a fixed 30 MHz crystal oscillator circuit and is not variable since the narrowest bandwidth selection for the 30 MHz IF is a width of 50 KHz, and the audio bandwidth of the receiver is only 20 KHz.

The amplitude modulated (AM) signal processing circuits include pulse stretch and slide back networks for both the 200 KHz and 30 MHz AM detectors. For slide back operation the front panel control is used to vary the video output signal from the AM detector, thus eliminating lower level signals and noise. The signal levels that are adjusted above a threshold level will illuminate the front panel slide back indicator.

When the pulse stretcher circuits are activated, they lengthen the pulse without changing the relative amplitude in order to obtain additional time to observe the detected video. Audio signals are separated from the detected output and routed to amplifier stages located on the A24 assembly. An audio stretch network using a fixed length, may be switch selected to allow very narrow audio pulses to be heard.

Frequency modulated signals are routed from the predetection amplifiers to the limiter/discriminator circuits which form the A9 assembly. In the FM mode, the individual limiter/discriminator networks are automatically selected depending upon the IF in use and the selected bandwidth. The detected output is applied through a video amplifier and routed to the FM video output connector. The amplified signal is filtered to separate the audio signal which is routed to the amplifier stage on the A24 assembly.

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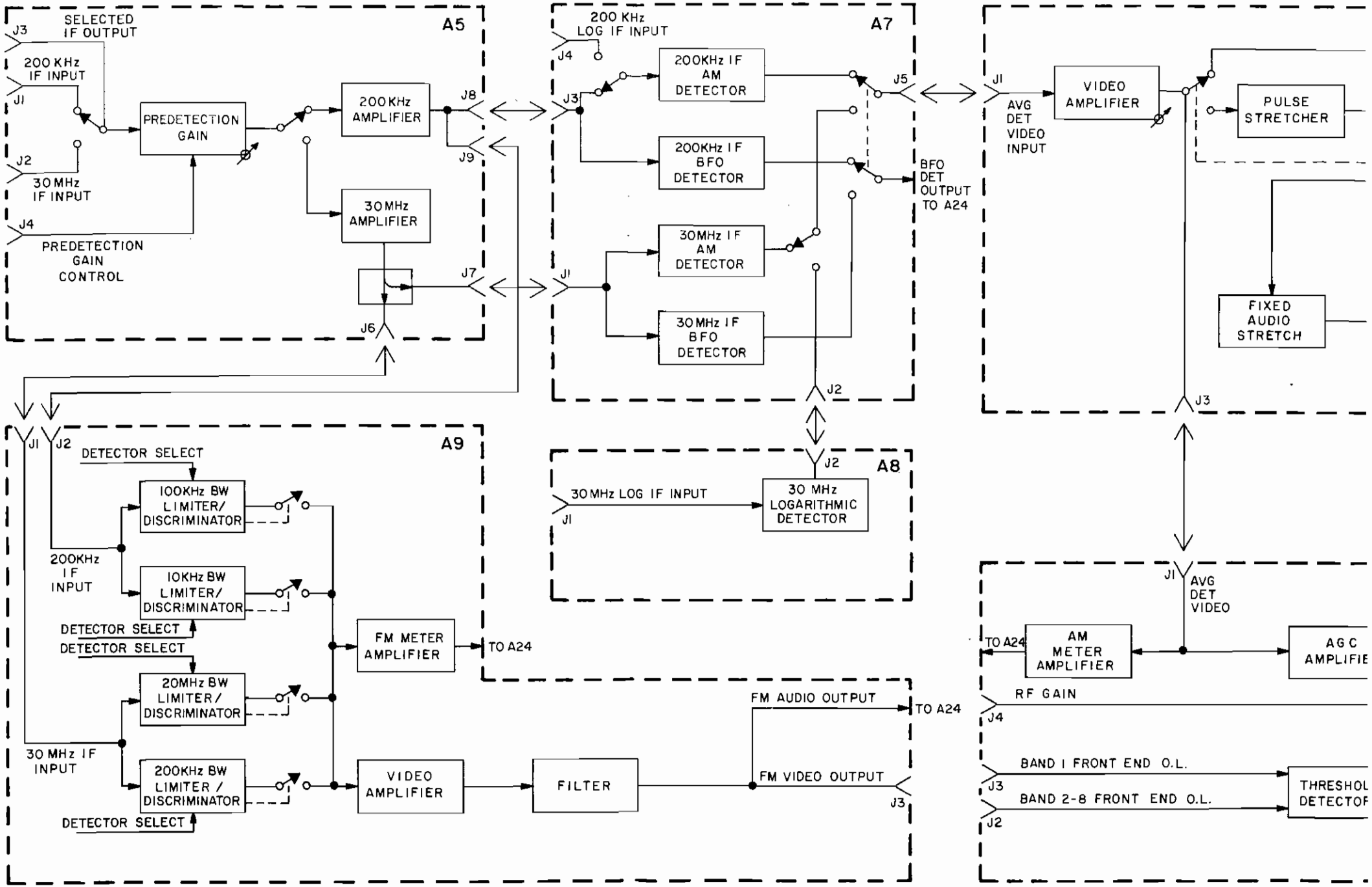
A5
SELECTED IF OUTPUT
J3
200 KHz IF INPUT
J1
J2
30 MHz IF INPUT
J4
PREDETECTION GAIN CONTROL
PREDETECTION GAIN
200 KHz AMPLIFIER
30 MHz AMPLIFIER
J8
J9
J7
J6
A7
200 KHz LOG IF INPUT
J4
J3
200KHz IF AM DETECTOR
200KHz IF BFO DETECTOR
30MHz IF AM DETECTOR
30MHz IF BFO DETECTOR
J5
BFO DET OUTPUT TO A24
J1
J2
A8
30 MHz LOG IF INPUT
J1
30 MHz LOGARITHMIC DETECTOR
J2
A9
J1
J2
DETECTOR SELECT
100KHz BW LIMITER/ DISCRIMINATOR
200KHz IF INPUT
10KHz BW LIMITER/ DISCRIMINATOR
DETECTOR SELECT
DETECTOR SELECT
20MHz BW LIMITER/ DISCRIMINATOR
30 MHz IF INPUT
200KHz BW LIMITER / DISCRIMINATOR
DETECTOR SELECT
FM METER AMPLIFIER
TO A24
VIDEO AMPLIFIER
FILTER
FM AUDIO OUTPUT
TO A24
FM VIDEO OUTPUT
J3
J1
AVG DET VIDEO INPUT
VIDEO AMPLIFIER
PULSE STRETCHER
FIXED AUDIO STRETCH
J3
J1
AVG DET VIDEO
TO A24
AM METER AMPLIFIER
AGC AMPLIFIE
RF GAIN
J4
BAND 1 FRONT END O.L.
J3
BAND 2-8 FRONT END O.L.
J2
THRESHOL DETECTOF

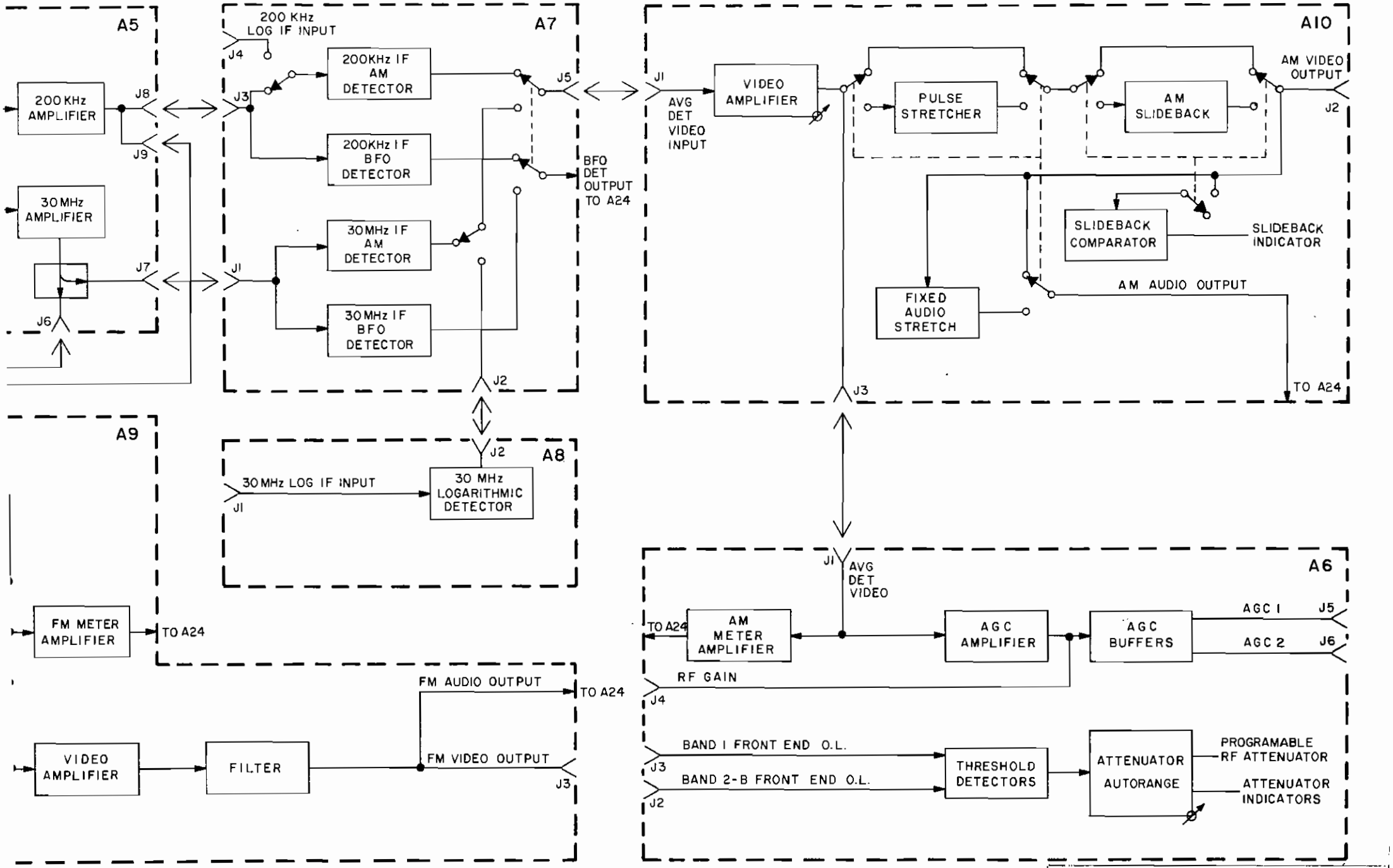

FIGURE 4-5 VIDEO SECTION BLOCK DIAGRAM
4-21/4-22

4.5 VIDEO SECTION (continued)

The A6 assembly contains the AGC amplifier and buffer circuits that generate the appropriate outputs (AGC 1 and 2), for application to the pin diode attenuator stages used in the IF amplifier strips. A delayed AGC is used so that the gain is not reduced by the attenuators near the front of the IF strip until the maximum gain reduction has been acheived by the attenuators located in the final stages of the IF strip, resulting in the best signal to noise ratio for varying signal conditions.

A front panel mounted RF gain control provides a variable output voltage that is a substitute for the outputs of the AGC circuits and is used when the manual gain position is selected. When either the FAST or SLOW AGC switch positions are selected, the RF gain control is used to override the automatic gain function, allowing manual variation of the receiver gain.

4.6 SYNTHESIZER SECTION

The frequency synthesizer, as shown in the diagram of figure 4-6, consists of individual printed circuit card assemblies and portions of the microwave assemblies that are part of the RF Section. The circuits within the synthesizer section generate and control both fixed and variable local oscillator frequencies, which are used in conversion stages to heterodyne receiver input frequencies into intermediate frequencies.

The theory of operation for the synthesizer section first covers the main LO which uses multiple phase locked loops to generate the variable frequencies, followed by the theory for individual circuits used to generate fixed frequency signals. All frequencies generated by the synthesizer are referenced to a precision crystal oscillator that produces a 1 megahertz signal which is routed to the A15 assembly for amplification and distribution.

4.6.1. MAIN LOCAL OSCILLATOR

The main LO consists of circuit card assembles A4, A12, A14, A16 and portions of the microwave assemble. Two configurations of phase locked loop circuits are used by the main LO: the single-loop/divide circuit that forms the A14 assembly, and the double-loop/mix and divide circuits that are used on the A12 and A16 assemblies.

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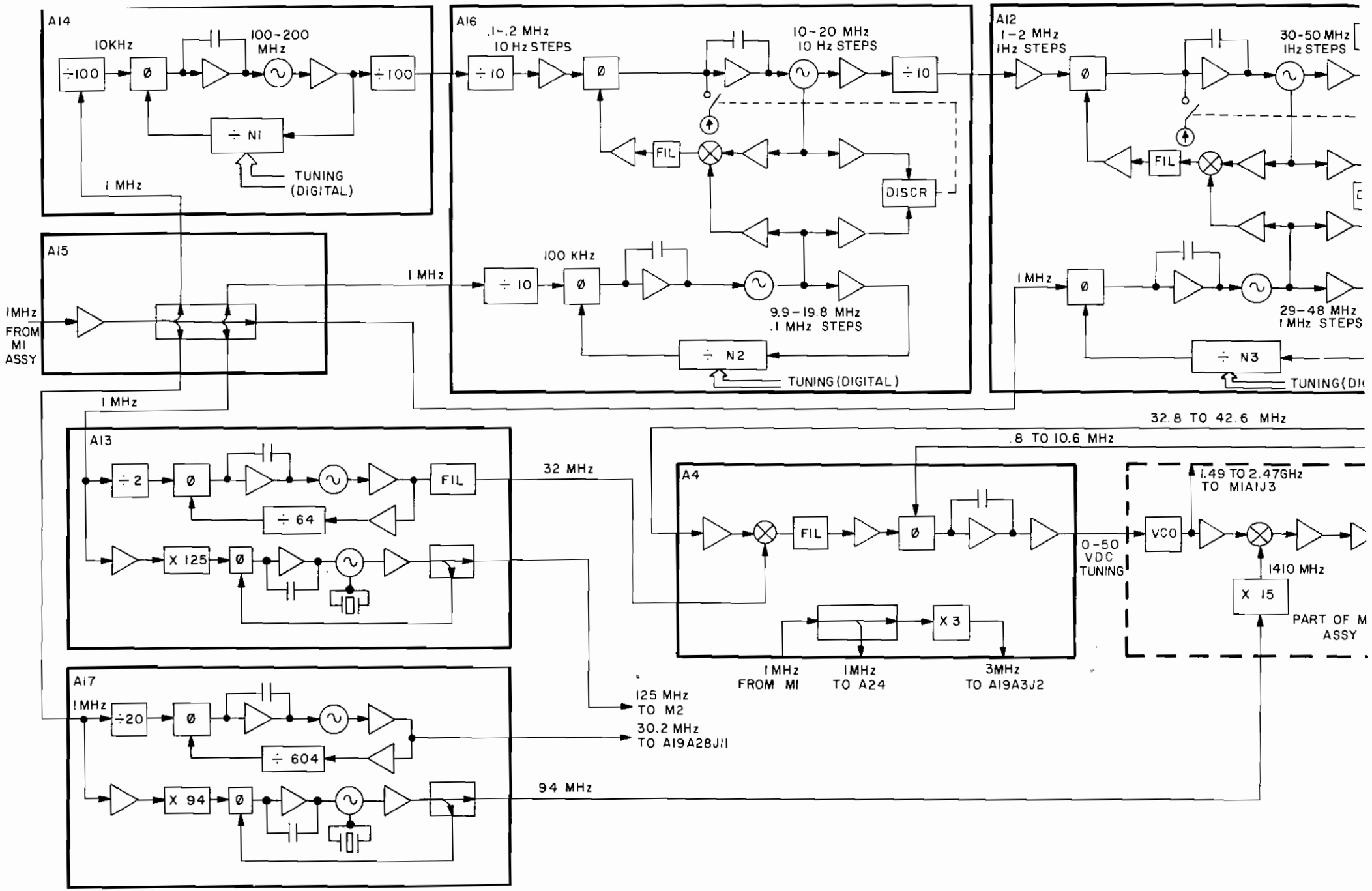
A14
10KHz
÷100
Ø
100-200 MHz
÷100
÷ N1
TUNING (DIGITAL)
1 MHz
A16
.1-.2 MHz 10 Hz STEPS
÷ 10
Ø
10-20 MHz 10 Hz STEPS
÷ 10
FIL
DISCR
100 KHz
÷ 10
Ø
9.9-19.8 MHz .1 MHz STEPS
÷ N2
TUNING (DIGITAL)
A12
1-2 MHz 1Hz STEPS
Ø
30-50 MHz 1Hz STEPS
FIL
1 MHz
Ø
29-48 MHz 1 MHz STEPS
÷ N3
TUNING (DI
A15
1MHz FROM MI ASSY
1 MHz
1 MHz
A13
÷ 2
Ø
FIL
÷ 64
X 125
Ø
40P
32 MHz
32.8 TO 42.6 MHz
.8 TO 10.6 MHz
A4
FIL
Ø
X 3
0-50 VDC TUNING
VCO
1.49 TO 2.47GHz TO MIAIJ3
1410 MHz
X 15
PART OF M ASSY
1MHz FROM MI
1MHz TO A24
3MHz TO A19A3J2
A17
1MHz
÷20
Ø
÷ 604
X 94
Ø
40P
125 MHz TO M2
30.2 MHz TO A19A28J11
94 MHz

FIGURE

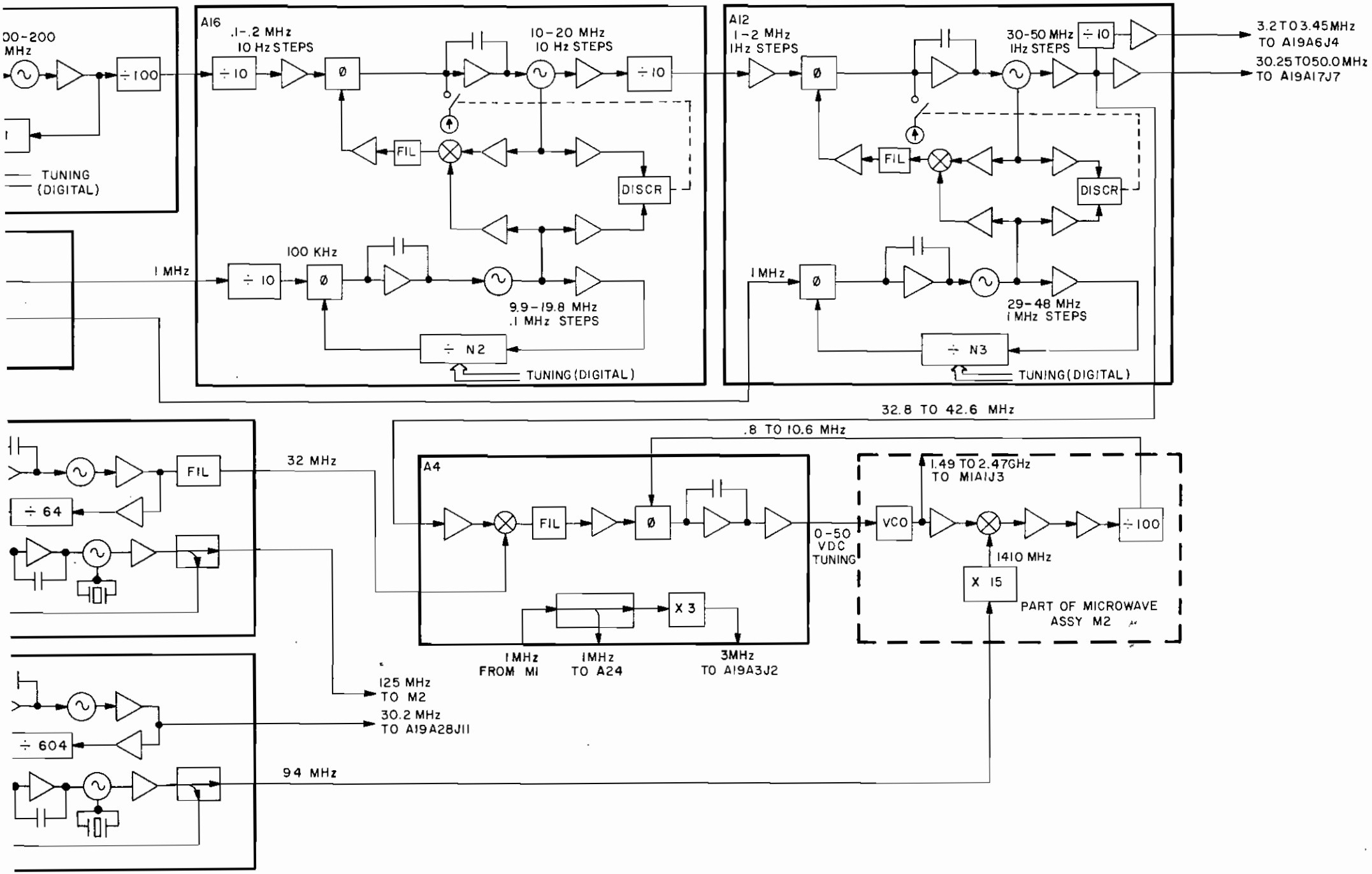

FIGURE 4-6 SYNTHESIZER SECTION BLOCK DIAGRAM
4-25/4-26

4.6.1. MAIN LOCAL OSCILLATOR(continued)

The single-loop/divide synthesizer circuit is based on a free-running voltage controlled oscillator (VCO) that generates an output ranging from 100 to 200 MHz. A divide- by-N1 prescaler converts a sample of the VCO output into a range that is equal to the prescaled value of the reference signal; in this case the 1 MHz reference is divided by 100 providing a 10 KHz signal. The tuning input to the N1 divider consists of the 16 bits from the 4 LEDs of the tuned receiver frequency. The fixed reference signal and the divided N1 tuning signal are routed to a phase/frequency detector that produces an error signal if the two inputs differ. The error signal is integrated, producing an increasing or decreasing drive voltage to the VCO. The output signal from the VCO is divided by 100 to produce and output range of 1 to 2 MHz that locks in 100 Hz steps and is coupled to the A16 assembly.

The circuits which form the A16 assembly consist of a double-loop/mix and divide synthesizer that is separated into two sections; a primary phase lock loop shown in the upper portion, and a secondary phase lock loop that operates identically to the single-loop/divide synthesizer of the preceding stage.

The secondary loop VCO generates a frequency across the range of 9.9 to 19.8 MHz which is slightly less than the frequency range of the primary loop VCO. The smaller frequency range is controlled by the divide-by-N2 tuning signal, whose binary weight represents the 3rd and 4th digit of the tuned receiver frequency. The output of the N2 divider is compared with the prescaled reference signal, which is 100 KHz, in the phase/frequency detector. The sense of the error signal produced by the detector drives an integrator which tunes the VCO in the direction required to obtain phase lock.

The primary phase lock loop is similar in operation, except the higher frequency range of this VCO is sampled and routed to a converter stage where it is mixed with the phase locked frequency of the secondary loop. The converted signal from the mixer is filtered and compared with the signal derived from the A14 assembly in a phase/frequency detector. Error signals produced by the phase detector are fed to an integrator which drives the VCO across its tuning range in 10 hertz steps . The VCO frequency is divided by 10, producing an output signal with a range from 1 to 2 MHz and a resolution of 1 Hz, that is routed to the A12 assembly.

To ensure that the primary loop frequency is always higher than the secondary loop frequency the two VCO signals are also sent to a discriminator. Should an input signal to the N2 divider cause the secondary loop VCO to be driven higher in frequency than the present output of the primary loop VCO, the discriminator senses the state of the two signals and activates a current source which drives the primary loop integrator, thus increasing the frequency of the 10 to 20 MHz VCO.

The operation of the A12 assembly is identical to that of the A16 assembly except the divide-by-N3 tuning signal represents the 2 MSD of the tuned receiver frequency. The double loop synthesis circuit for this portion of the main LO provides three separate outputs. Each output is within the range of 30 to 50 MHz, but shown on the block diagram as the exact frequency range used by the respective conversion stages.

The first output (F6) is divided by 10 to produce a frequency ranging from 3.2 to 3.45 MHz. This signal has a resolution of .1 Hz and is used in the second mixer stage of the band 1 converter. The second frequency (F3) output has a range from 30.25 to 50.0 MHz with a resolution of 1 Hz and is used in the first mixer stage for conversion of band 2 frequencies (see figure 4-4).

The remaining variable frequency generated by the A12 assembly ranges from 32.8 to 42.6 MHz and is routed to the A4 assembly. The circuits contained on the A4 assembly and those that are part of the RF section, provide the control signals and the lock loop for the microwave local oscillator frequency ranging from 1.49 to 2.47 GHz. The microwave LO signal is used by the first mixer stage in the RF section which produces the 1470 MHz intermediate frequency.

The microwave LO signal, designated F1, is generated by a free-running VCO. A sample of the VCO signal is down converted by mixing with a fixed frequency of 1410 MHz. This fixed frequency is produced by multiplying a fixed 94 MHz that is generated on the A17 assembly. The down converted signal is amplified and divided by 100 to derive a phase comparison signal ranging from .8 to 10.6 MHz. The remaining comparison signal, which must also range from .8 to 10.6 MHz, is developed by mixing the variable frequency of 32.8 to 42.6 MHz with a fixed 32 MHz signal from the A13 assembly. The down-converted signal is filtered to remove any harmonic components and routed for comparison to a phase/frequency detector.

Any error signal produced by the phase difference of the two signals drives an integrator which produces a 0 to 50 volt DC drive signal to the VCO, increasing or decreasing the frequency until phase lock is obtained.

4.6.2 FIXED FREQUENCY OSCILLATORS

Four individual phase locked loop circuits are used to generate fixed frequencies. The A13 assembly contains synthesizer loops which generate a 32 MHz signal and the 125 MHz signal. The 125 MHz signal is subsequently multiplied and used in conversion stages that produce the 30 MHz IF. The 32 MHz signal is produced by a VCO whose output is filtered and routed to the A4 assembly. A portion of the VCO signal is sampled and divided by 64 to provide a 500 KHz signal that is phase compared with a prescaled reference digital frequency. Any variation in the VCO frequency produces a phase error that is integrated, driving the VCO in the direction required to maintain phase lock. The 125 MHz signal is also generated by a single loop synthesizer except that frequency is phase locked to a voltage controlled crystal oscillator (VCXO). The VCXO frequency is sampled and fed directly to a phase frequency detector. Since the two input signals to the detector must be at the same frequency, the 1 MHz reference signal is multiplied by 125 and compared with the crystal frequency to produce an error signal that drives an integrator.

The phase locked loops that generate the fixed frequencies of 30.2 MHz and 94 MHz are identical to those contained on the A13 assembly with the exception of the prescaled values used to derive frequency comparison signals. The 94 MHz signal is routed to the RF section as previously discussed. The fixed 30.2 MHz signal is designated F4 and is used by the second mixer stage of the 30 MHz IF for conversion of signals within bands 2-7 that have a selected bandwidth less than 50 KHz.

4.7 DIGITAL SECTION

The major assemblies of the digital section are shown in the block diagram of figure 4-7. The digital circuits provide the timing and control of the various functions within the receiver for both manual and automatic modes of operation. Manual functions from the front panel controls and auto functions carried over the IEEE-488 interface bus are converted into digital formats that are used to control the displayed frequency, status indicators, band/bandwidth functions and the frequency tuning data used by the synthesizer circuits.

The digital section consists of three major assemblies: the IEEE bus interface (A23), the control and switching logic circuits (A11), and the front panel logic assembly (A24). The bus interface circuits and the control and switching logic are each contained on individual printed circuit assemblies located in a card cage. The front panel logic circuits include the front panel mounted controls and indicators, along with a printed circuit assembly that is mounted behind the front panel and interconnects with other circuits over dedicated wires.

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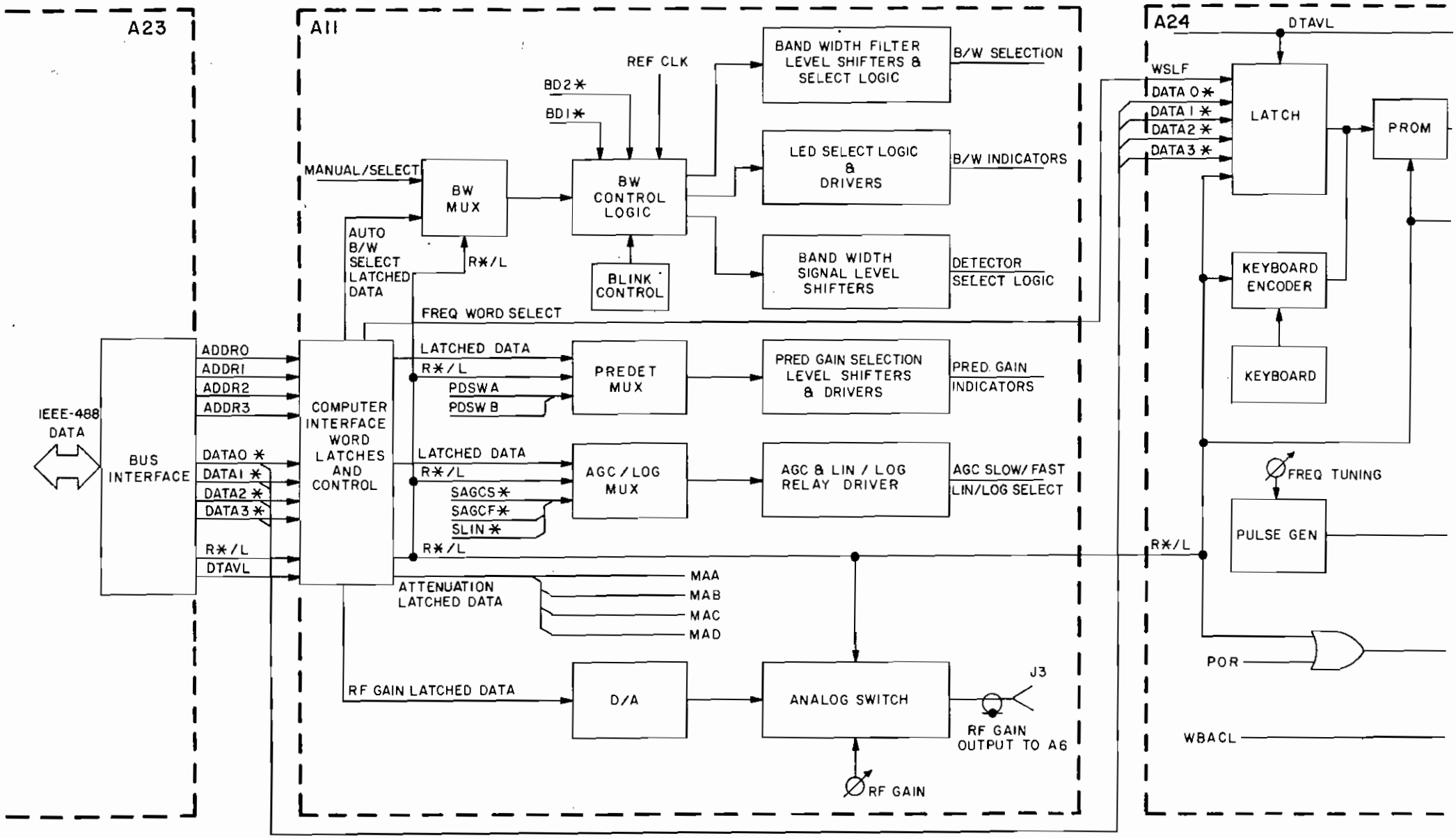
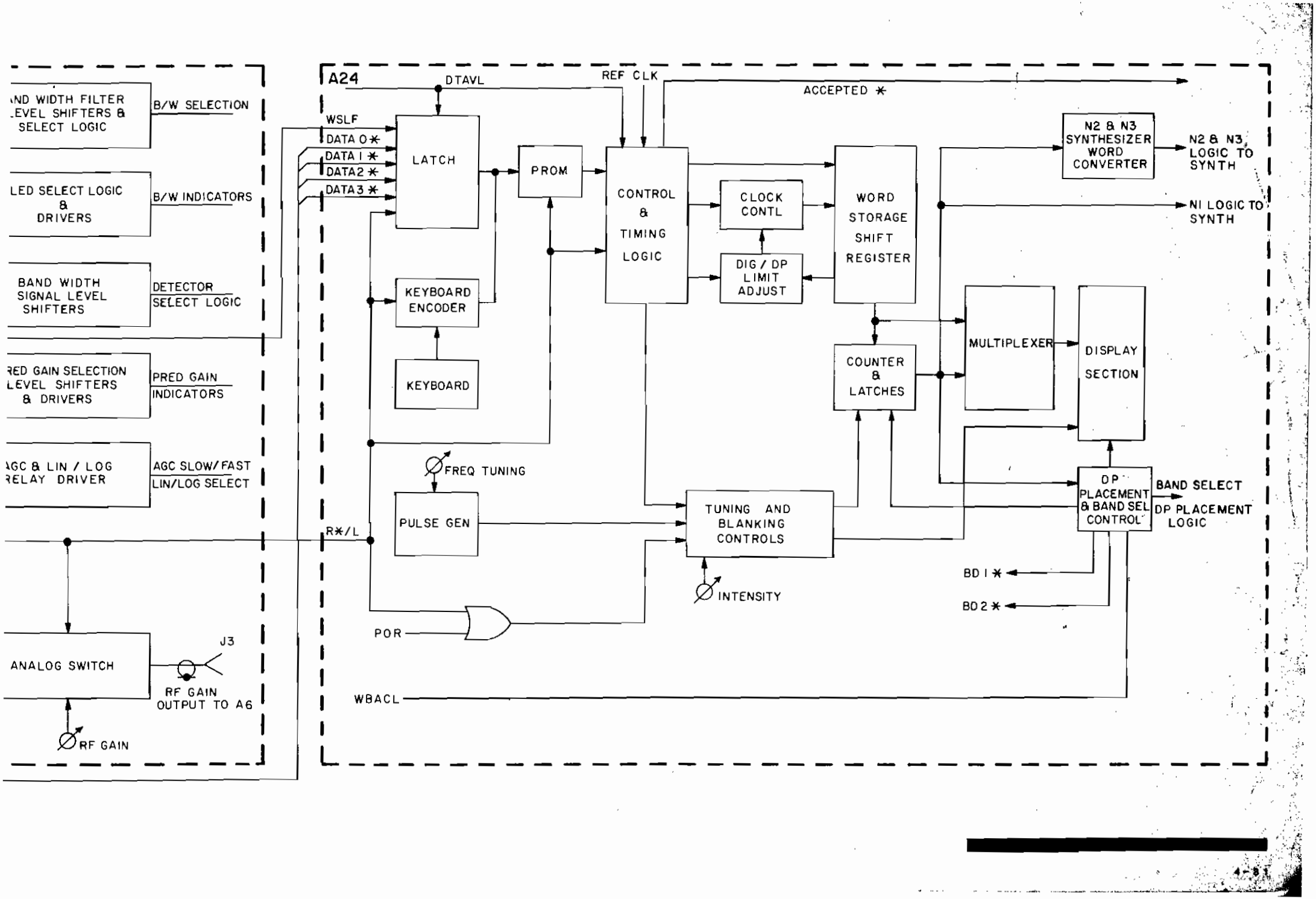

A23
A11
A24
IEEE-488 DATA
BUS INTERFACE
ADDR0
ADDR1
ADDR2
ADDR3
DATA0 *
DATA1 *
DATA2 *
DATA3 *
R*/L
DTAVL
COMPUTER INTERFACE WORD LATCHES AND CONTROL
MANUAL/SELECT
BW MUX
AUTO B/W SELECT LATCHED DATA
R*/L
BD2*
BD1*
REF CLK
BW CONTROL LOGIC
BLINK CONTROL
BAND WIDTH FILTER LEVEL SHIFTERS & SELECT LOGIC
B/W SELECTION
LED SELECT LOGIC & DRIVERS
B/W INDICATORS
BAND WIDTH SIGNAL LEVEL SHIFTERS
DETECTOR SELECT LOGIC
FREQ WORD SELECT
LATCHED DATA
R*/L
PDSWA
PDSW B
PREDET MUX
PRED GAIN SELECTION LEVEL SHIFTERS & DRIVERS
PRED. GAIN INDICATORS
LATCHED DATA
R*/L
SAGCS*
SAGCF*
SLIN*
AGC/LOG MUX
AGC & LIN / LOG RELAY DRIVER
AGC SLOW/FAST
LIN/LOG SELECT
R*/L
ATTENUATION LATCHED DATA
MAA
MAB
MAC
MAD
RF GAIN LATCHED DATA
D/A
ANALOG SWITCH
J3
RF GAIN OUTPUT TO A6
RF GAIN
DTAVL
WSLF
DATA 0*
DATA 1*
DATA2*
DATA3*
LATCH
PROM
KEYBOARD ENCODER
KEYBOARD
FREQ TUNING
PULSE GEN
R*/L
POR
WBACL


ND WIDTH FILTER
EVEL SHIFTERS &
SELECT LOGIC
B/W SELECTION
LED SELECT LOGIC
&
DRIVERS
B/W INDICATORS
BAND WIDTH
SIGNAL LEVEL
SHIFTERS
DETECTOR
SELECT LOGIC
RED GAIN SELECTION
LEVEL SHIFTERS
& DRIVERS
PRED GAIN
INDICATORS
AGC & LIN / LOG
RELAY DRIVER
AGC SLOW/FAST
LIN/LOG SELECT
ANALOG SWITCH
J3
RF GAIN
OUTPUT TO A6
RF GAIN
A24
DTAVL
REF CLK
ACCEPTED *
WSLF
DATA 0 *
DATA 1 *
DATA2 *
DATA3 *
LATCH
PROM
CONTROL
&
TIMING
LOGIC
CLOCK
CONTL
DIG / DP
LIMIT
ADJUST
WORD
STORAGE
SHIFT
REGISTER
N2 & N3
SYNTHESIZER
WORD
CONVERTER
N2 & N3
LOGIC TO
SYNTH
NI LOGIC TO
SYNTH
KEYBOARD
ENCODER
KEYBOARD
COUNTER
&
LATCHES
MULTIPLEXER
DISPLAY
SECTION
FREQ TUNING
PULSE GEN
R*/L
TUNING AND
BLANKING
CONTROLS
DP
PLACEMENT
& BAND SEL
CONTROL
BAND SELECT
DP PLACEMENT
LOGIC
INTENSITY
BD 1 *
BD2 *
POR
WBACL

4.7 DIGITAL SECTION (continued)

The bus interface assembly contains circuits that provide the timing logic required for the automatic data control signals which interface with the receiver over the IEEE-488 General Purpose Interface Bus (GPIB). Descriptions and specifications for the bus are contained in the IEEE standard for programmable instrumentation, "IEEE Std. 488-1978".

Bus interface data is sent to the control and switching logic circuits and is loaded into computer interface word latches. The latches are enabled by the state of the R*/L (Remote/Local) line. The data lines provide the input logic to the word latches and are controlled by the address lines that determine which latches will be strobed depending on the state of the DTAVL (data valid) line. Latched data is sent to the various function multiplexers and a D to A (digital-to-analog) conversion stage.

Input data to each multiplexer is derived from either the computer interface circuits, when using the auto mode, or from signals generated by the front panel controls when in the manual mode. The mode of operation determines the status of the R*/L line.

Multiplexed bandwidth selection data is applied to the bandwidth control circuits which use a series of combinational logic and PROM resident look-up tables to generate the specific function codes. The unique codes derived from the control circuits determine the bandwidth selected, the state of the BW indicators, the position of each frequency band selection relay, and the detector/discriminator select logic. In addition to the multiplexed bandwidth selection and control logic, individual multiplexers are used to provide predetection gain selection and the selection of AGC logic along with linear or logarithmic functions.

RF gain latched data is converted into a DC voltage by the digital to analog conversion stage. The DC voltage is used to control an analog switch which provides selection of either a computer controlled analog signal or a variable DC signal derived from the front panel mounted RF gain control.

Data lines from the bus interface circuits of the A23 assembly are also routed to separate latch circuits on the front panel logic assembly (A24). The state of the R*/L logic determines the use of either latched data from a remote source or keyboard encoded data from the front panel. The selected data source provides the preprogrammed coded output from the read-only-memory which is sent to control and logic timing circuits.

Coded data corresponding to digit entries and decimal point location selection are routed to the word storage shift registers and sequentially loaded. The loaded data is monitored by the DIG/DP (digit/decimal point) limit adjust logic which issues a single clock pulse for each load sequence. The output from the shift registers is multiplexed providing drive signals to the display section and is also loaded into a counter/latch circuit which holds the bit pattern until the termination logic (MHz or KHz) is loaded, at which time the DIG/DP limit circuit issues the appropriate number of clock pulsed based on an interrogation of the shift registers.

Each time new frequency values are entered and encoded, the shift registers provide new bit pattern information to the counter/latch circuits. The data from the counter/latch circuits provides updated multiplexed display values and also provide band selection logic and new N1, N2 and N3 synthesizer words.

Increment and decrement logic drives a counter in the tuning and blanking control circuits, thus selecting one of five digits that will respond to the pulse generator output controlled by the frequency tuning knob. The blanking control circuit issues a blanking pulse to the display causing the selected digit to blink at a fixed rate. The pulse generator controlled by the frequency tuning knob produces TTL logic signals that are rotation sensitive. The pulse output is sent to the tuning and blanking circuits which in turn drive the counter/latch stage which determines the direction of rotation and the resulting increase or decrease of the selected digit location.

4.8 POWER SECTION

The Power Supply section includes a regulator assembly and a separate plug-in module that provides conversion of the input source power into five unregulated direct current levels. A combination of bridge rectifiers and filter networks produce the unregulated voltages which are routed to individual regulation circuits that provide the operating voltages for the receiver.

The block diagram of figure 4-8 shows the unregulated voltages produced by the rectifier/filter stages and the routing of these DC levels to the individual regulator networks. Each regulated output, with the exception of the +28 VDC, is independently adjustable and includes a rear panel mounted light emitting diode that indicates voltage output.

The plus and minus 15 VDC, the plus and minus 12VDC, and both plus 5VDC regulator outputs are fed into crowbar networks. Each circuit is individually adjusted to a predetermined trigger level that shuts down the regulator if its output exceeds the preset limit.

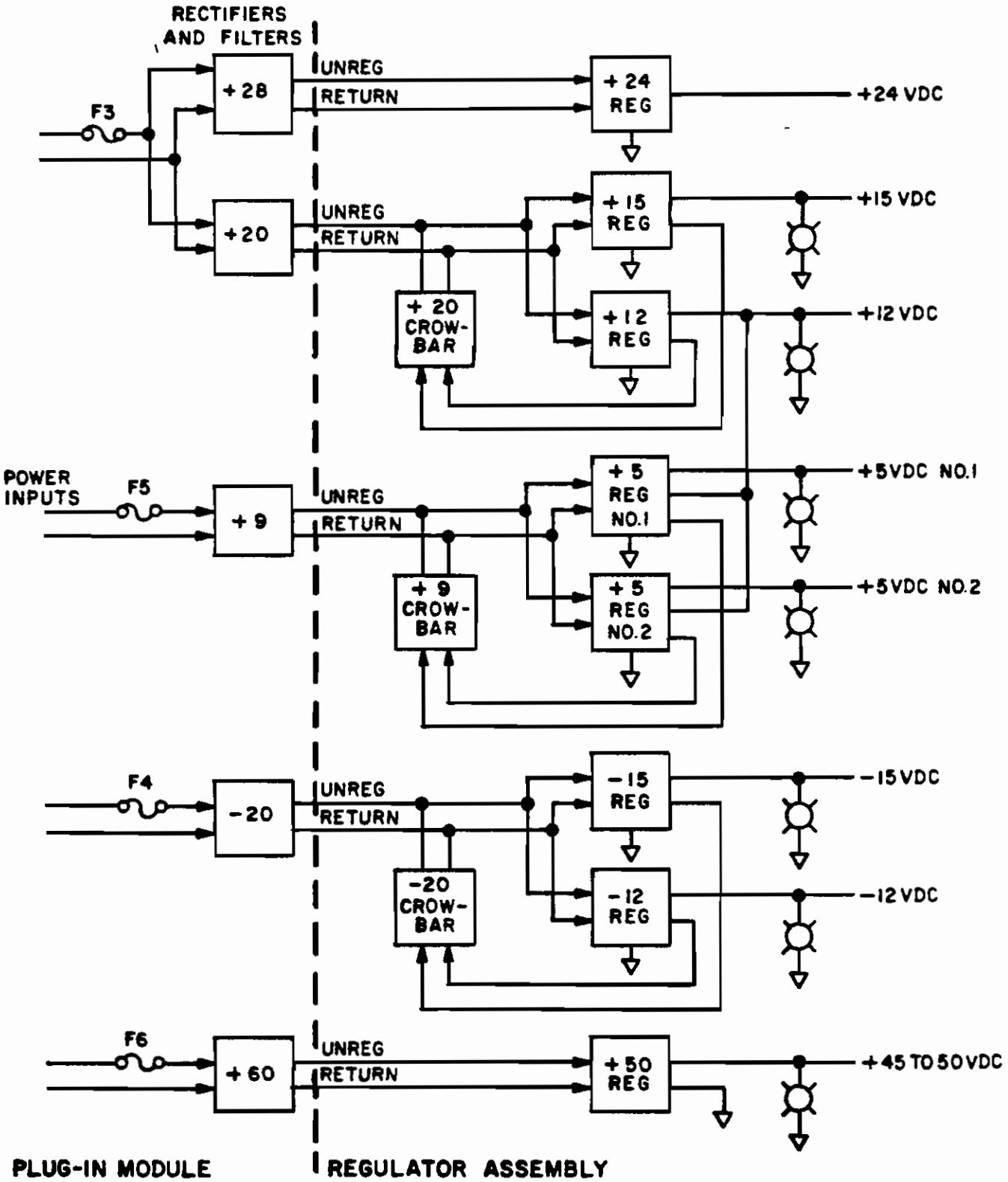


FIGURE 4-8 POWER SECTION BLOCK DIAGRAM

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