# Introduction to Computer Architecture: Supervision 2

Lectures covered by the supervision: https://www.cl.cam.ac.uk/teaching/2526/IntComArch/

- Lecture 5: Executable processor models
- Lecture 6: Processor pipelines – part I
- Lecture 7: Processor pipelines – part II
- Lecture 8: Memory hierarchy

Past exam questions:
https://www.cl.cam.ac.uk/teaching/exams/pastpapers/t-ComputerDesign.html

Supervision questions:

1. Explain the process from designing RTL to manufacturing chips. What is the role of Electronic design automation (EDA) tools in this process?
2. 2018 Paper 5 Question 2 - parts a, b, e.
3. Discuss ISA-level simulation with an example. How would you verify if your processor conforms to a specific ISA?
4. What is the difference between data-path and control-path, and why do they tend to flow together down the pipeline?
5. Pick one RISC-V and one ARM instruction. Explain its encoding, registers affected by that instruction, and its logic.
    a. Hints:
        i. https://riscv.org/technical/specifications/
        ii. https://developer.arm.com/documentation/ddi0487/latest/
6. 2017 Paper 5 Question 2.
7. Does a CPU have a view of an application? Explain the process of starting an application on a CPU (which registers need to be populated). How is the compilation process relevant to this?
8. Do pipelines always have five stages? Does ISA define the number of pipeline stages?
9. 2016 Paper 5 Question 2.
10. Discuss in-order vs out-of-order execution of instructions. Which one tends to provide better performance? Why?
11. 2021 Paper 5 Question 2 – part a, c.
12. 2019 Paper 5 Question 2 - parts a, b, c, d.
13. 2009 Paper 5 Question 3 - parts b, c, d.
14. What is cache miss rate and why must it be very low if it is not to have a major negative impact on processor performance? What would happen if we would decide not to use cache – are there any positive side-effects?
15. Discuss a case in which pipelining can make execution of a single instruction slower and the execution of a set of instructions faster?
16. What are the sources of cache misses and what is their influence on variation of execution time?
17. Summarize the main message from lesson 5 in 1-3 sentences?
18. Summarize the main message from lesson 6 in 1-3 sentences?
19. Summarize the main message from lesson 7 in 1-3 sentences?
20. Summarize the main message from lesson 8 in 1-3 sentences?

Bonus:

21. Discuss in-memory computation.
22. Create an example in https://github.com/swm11/riscv-lite/tree/master/jsim

Save your answers into MS Teams or email them to me. Please use the following naming pattern:

ICA_Supervision_2_Answers_<last name>_<first name>_Michaelmas_2025

Send your answers as a pdf, doc, image, or any other format of a document for which there exists an easily available software to open.

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