Introduction to Computer Architecture: Supervision 3

Lectures covered by the supervision: [https://www.cl.cam.ac.uk/teaching/2223/IntComArch/](https://www.cl.cam.ac.uk/teaching/2223/IntComArch/)

- Lecture 9: Support for operating systems. Memory protection, exceptions, interrupts, etc.
- Lecture 10: Other instruction set architectures. CISC, stack, accumulator
- Lecture 11: Overview of Systems-on-Chip (SoCs) and DRAM. High-level SoCs, DRAM storage and accessing.
- Lecture 12: Multicore Processors. Communication, cache coherence

Past exam questions:

Supervision questions:
1. What are the differences between interrupts, environment calls (software interrupts), and exceptions?
2. 2008 Paper 6 Question 2 - part a
3. 2006 Paper 6 Question 2 - part b
4. Sketch examples of a i) memory read and a ii) memory write, former cache hit, latter cache miss, considering a processor with a single level of cache, virtual memory (TLB, page table), and RAM. Explain both examples.
5. How does a Translation Look-aside Buffer TLB improve performance of virtual memory accesses?
6. How is virtual memory used to isolate applications?
7. What are the main components of a modern SoC?
8. Suppose that there are four different types of processor: A does 15% of the work for an application, B does 20%, C does 5% and D does 60%. If you speed B up by 2× and D up by 3×, what is the overall application speed up:
   a. When all four run in parallel?
   b. When all four run sequentially?
   c. What’s the limit on the speedup you can get from only improving B and D?
9. Draw a 1T1C DRAM cell. Why does it need refresh and what is it?
10. A memory controller converts processor requests into commands for the DRAM.
    a. Why might it prefer to order requests so that they access different banks on consecutive memory operations, rather than the same bank?
    b. When is it beneficial to continuously access the same bank?
11. Why is there a need to perform both a row access and column read when reading data out of DRAM? What does each operation do?
12. Describe the four classes in Flynn’s taxonomy of computing systems. Explain where a multicore processor with a short-vector instruction set fits within Flynn’s taxonomy?
13. Describe Amdahl’s and Gustafson's law. Comment what is happening as we increase the number of cores in case as observed by Amdahl – how realistic it is to see the predicted results in real-world applications?
14. Show, with the aid of a diagram, how DRAM is organised, making reference to devices, ranks, banks and arrays.
15. Describe the difference between an open-page and closed-page row-buffer policy and the types of access patterns they benefit.
16. Why is shared memory a useful concept for programmers? Describe its disadvantages.
17. Considering discussed shared cache organisations, what are the benefits and downsides to each approach?
18. Describe inclusive, exclusive and non-inclusive cache policies.
a. Can you develop a set of examples to demonstrate that under certain conditions one policy can outperform all others?

19. Describe MSI cache coherence protocol. Can you think of a software example/application problem where this becomes a bottleneck?

20. You hold data at address X when you snoop a BusRd transaction from the bus. What actions do you take with the MSI cache coherence protocol if you start in:
   a. State M?
   b. State S?
   c. State I?


22. Summarize the main message from lesson 9 in 1-3 sentences?

23. Summarize the main message from lesson 10 in 1-3 sentences?

24. Summarize the main message from lesson 11 in 1-3 sentences?

25. Summarize the main message from lesson 12 in 1-3 sentences?

Save your answers into MS Teams or email them to me. Please use the following naming pattern:
ICA_Supervision_3_Answers_<last name>_<first name>_Michaelmas_2022

Send your answers as a pdf, doc, image, or any other format of a document for which there exists an easily available software to open.

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