Jianyi Cheng University of Cambridge, UK jianyi.cheng@cl.cam.ac.uk

Christos-Savvas Bouganis Imperial College London, UK christossavvas.bouganis@imperial.ac.uk Cheng Zhang Imperial College London, UK cheng.zhang122@imperial.ac.uk

George A. Constantinides Imperial College London, UK g.constantinides@imperial.ac.uk Zhewen Yu Imperial College London, UK zhewen.yu18@imperial.ac.uk

Yiren Zhao Imperial College London, UK a.zhao@imperial.ac.uk

ABSTRACT

Model quantization represents both parameters (weights) and intermediate values (activations) in a more compact format, thereby directly reducing both computational and memory cost in hardware. The quantization of recent large language models (LLMs) faces challenges to achieve competitive memory density compared to other models such as convolutional neural networks, since values in LLMs require larger dynamic ranges.

Current hardware can expedite computation for LLMs using compact numerical formats such as low-bitwidth integers or floatingpoint numbers. Each has advantages: integer operations simplify circuit design, whereas floating-point calculations can enhance accuracy when a wider dynamic range is required. In this work, we seek an efficient data format that combines the best of both worlds: Microscaling (MX) formats. MX formats are efficient data formats that achieve both large dynamic ranges and high memory density.

In this paper, we propose a compiler named MASE for exploring mixed-precision MX formats on dataflow hardware accelerators for LLM inference. Our main contributions are twofold. First, we propose a novel orchestration abstraction to explore both software and hardware optimizations with new data formats. Second, MASE achieves LLM inference at an average precision of 4-bits, with minimal to no accuracy degradation. To our knowledge, MASE represents the first effort to harness fine-grain multi-precision MX formats in the design of LLM hardware accelerators. Over a range of LLMs and datasets, MASE achieves an average improvement of 24% in Δ accuracy with an overhead of only 3% in energy efficiency compared to designs using 8-bit fixed-point numbers.

1 INTRODUCTION

Large Language Models (LLMs) [4, 5, 8, 54, 55, 71] have gained significant attention, with empirical evidence suggesting that models must reach a certain scale to exhibit *emergent abilities* [59]. These large models, such as GPT-3, Vicuna and LLaMA, are pre-trained on vast amounts of text data, enabling them to provide state-ofthe-art results in areas like language translation [23], questionanswering [63], sentiment analysis [40]. One of the main challenges in LLM inference is the vast number of parameters involved [69]. For example, the larger variants in the GPT family can have hundreds of billions of parameters, which would require a minimum of 300 GB of memory to store them in a FP16 format [5]. To reduce memory size, quantization is employed to reduce the precision of Table 1: Evaluation of MX formats in similar average bits for quantizing LLaMA on Wikitext2. Small perplexity means better LLM performance. Higher memory density or hardware arithmetic density (both defined by Darvish *et al.* [14]) means better hardware efficiency.

Approaches	Config	Perplexity	Memory Density	Arithmetic Density
FP32	-	7.06	$1 \times$	1×
Int8	W8A8	265	$4 \times$	7.7×
FP8	W8A8	7.18	$4 \times$	17.4×
MXInt8	W8A8	7.07	3.8×	14.4×
BMF8	W8A8	223k	3.8×	$14.4 \times$
BL8	W8A8	18.8	3.8×	16.1×

both model parameters and activations to a more compact representation.

Background: Large numerical variation in activation values motivates quantization with new data formats for efficient LLM inference. Existing LLM hardware accelerator designs typically quantize each tensor into one of two common number representations: fixed-point formats, such as int8, and floatingpoint formats, such as FP8. Both representations have their merits: operations with fixed-point formats simplify circuit design, while operations with floating-point formats can enhance accuracy when a wider dynamic range of value is required. LLM quantization is more challenging because it has both a large variation of values and high computational complexity. For example, the variance of all activations in each transformer block of LLaMA averaged across all data points in the Wikitext2 dataset is plotted in Fig. 1a. This plot highlights that the variances change drastically for different tensors in different layers. For example, variances increase in deeper layers with significant changes up to $7624 \times$ (the variable *D* in Fig. 1a). Also, variances significantly vary between tensors, even if they are within the same layer; for example, A and D exhibit a 7902-fold variance difference at layer 0. This observation motivates us to explore efficient data formats that combine the best of both worlds of fixed-point and floating-point formats.

Design Opportunities: Microscaling (MX) formats have shown initial promising results in LLM quantization. MX formats are a class of data representations that allow a block of values



activation in an LLM have dis- across blocks when

tinct distributions cross dif-quantized to mixed-(c) Examples of FP8 and (d) The dataflow graph of a transformer block (f) A schedule of the block for a ferent layers. mixed-(c) mixed-(c

Figure 1: An example of mapping LLaMA onto a dataflow accelerator. The large variances of each activation cross different layers in (a) motivate us to use quantization with MX formats in (c). We achieve mixed-precision quantization in (b) and map the model onto a dataflow architecture in (d). The dataflow schedule exploits task-level parallelism in (f), leading to a higher throughput compared to a non-dataflow schedule in (e). The proposed MASE compiler provides a fully automated and efficient approach to exploring software and hardware optimizations for MX formats.

to share certain components of their data formats, as illustrated in Fig. 1c, leading to efficient memory size. Table 1 gives a comparative overview of different MX formats against other arithmetic types when prototyped on FPGAs. Among all data formats, the MXInt format, a subclass of MX formats, offers an advantage in achieving a favorable balance between minimizing accuracy loss and optimizing hardware efficiency.

Problem: Existing approaches require manual effort to explore custom data formats for LLM accelerator designs. Although MX formats have recently been standardized by AMD, Arm, Intel, Meta, Microsoft, NVIDIA, and Qualcomm [44], the exploration of MX formats on hardware accelerators remains limited. A major reason is that there is no tool available to explore these formats for hardware accelerator designs. In practice, significant manual effort is spent on iterations between software model and hardware mapping to determine an optimized co-design. Existing work on MX quantization treats each layer equally and applies the same quantization to all tensors [14, 49]. This reduces the design space but also misses opportunities to perform model-specific optimizations for a given LLM, potentially making the optimal hardware design unreachable.

In order to tackle the problems above, our work aims to solve the following challenges:

1) Efficiency: How should one efficiently explore fine-grained quantization of an LLM using custom data formats?

2) Hardware awareness: How should one determine a quantization solution that leads to an efficient hardware design?

The efficiency here means minimal design effort, avoiding re-implementing optimizations from scratch for a new data format. Existing optimization algorithms originally for existing data formats may be reused to explore design opportunities for new data formats. These optimizations must take hardware intrinsics into account, leading to a hardware-friendly solution.

Solution: We propose a novel co-design compiler named MASE to explore custom MX formats for efficient LLM inference on dataflow accelerators. Specifically, MASE provides an efficient co-design intermediate representation (IR) named MASE IR to explore software and hardware co-design with custom data formats. A key novelty of MASE IR is that it orchestrates existing optimization techniques for traditional data formats to explore hardware optimization opportunities for custom data formats. To efficiently exploit fine-grained mixed-precision custom MX quantization, MASE maps an LLM onto dataflow architectures where each tensor precision can be tailored at the bit level.

To our knowledge, MASE is the first approach to dataflow hardware design using mixed-precision MX formats. Our main contributions are as follows:

 an end-to-end compiler that automatically determines a mixed-precision MX quantization for a given LLM for mapping onto an efficient dataflow hardware accelerator;

- an efficient orchestration method using a co-design IR to explore both software and hardware designs for custom data formats such as MX formats;
- an open-source library of parameterized hardware operator designs using MX formats and their evaluation model at the source level for mixed-precision quantization search and efficient hardware generation; and
- over a set of LLM families and datasets, our approach attains on average 24% in ∆ accuracy with an overhead of 3% in area efficiency compared to designs using 8-bit fixed-point numbers.

The rest of the paper is organized as follows. Section 2 provides a motivating example for exploiting custom MX formats in LLM hardware accelerator design; Section 3 describes MASR IR and its optimization orchestration; Section 4 describes our modeling of MXInt formats for efficient quantization search; Section 5 evaluates our design over a set of state-of-the-art LLM models; and Section 6 reviews related work on block-based quantization, hardware compilers for LLM inference, and hardware accelerator designs.

2 MOTIVATING EXAMPLE

In this section, we begin by introducing dataflow hardware architectures and their optimization opportunities for fine-grained quantization. We also provide an overview of three MX formats and evaluate their performance in quantizing LLMs.

Why Dataflow Accelerators? Dataflow hardware accelerators are specialized hardware architectures that drive operations using the presence of input data, leading to parallelized execution of coarse-grained tasks across several spatial processors. Fig. 1e illustrates a schedule running on a non-dataflow architecture, such as Von-Neumann architecture, where only one task is executed at a time. This means that all the hardware resources are exploited for each task, leading to a low latency, however, these tasks are sequentially executed in time. On the other hand, a dataflow architecture exploits spatial parallelism among these tasks, leading to a schedule in Fig. 1f. Such a parallelism, also known as pipelining, leads to high data throughput, however, the latency is sub-optimal since the hardware resources are shared among different tasks.

We focus on dataflow architectures because each spatial processor can be tailed for the task that it computes, while non-dataflow architectures require general spatial processors for all tasks. This leads to minimal instruction overhead and design opportunities for fine-grained customization down to the bit level. Targeting a dataflow architecture allows us to simplify the hardware design problem, such as excluding control flow design, and focus on dataspecific hardware optimizations.

For example, Fig. 1d illustrates a transformer block of LLaMA mapped onto a dataflow architecture. In an LLM, tensors are often large, and their computation cannot be fully parallelized for given available hardware resources. Instead, they are partitioned into tiles and streamed into the hardware in a deep pipeline. The streaming orders of these tiles depend on the dataflow hardware operator behaviors. In the figure, tensors are streamed either in a row-by-row or column-by-column order. There are also dataflow-specific operators in the hardware, such as 'transpose' and 'reorder', to switch the streaming order in between at run-time. In this work, we take

this hardware architecture as a starting point, and explore efficient mixed-precision quantization search at the tensor level using MX formats. For example, Fig. 1b illustrates the bitwidth distribution of the activations and weights in Fig. 1a across transformer blocks using our work.

What are MX Formats? MX formats allow a block of values to share certain components of a data format as a scaling factor [44]. The scaling factor enables individual values to represent larger dynamic ranges compared to traditional integers. The elements then provide a high-precision representation of values within the range specified by the scaling factor. MX formats could further reduce the average bits per value due to the sharing of the scaling factor in the block. A key requirement is that all the elements in a block must be within the same range specified by the scaling factor.

By means of examples, we compare three MX formats with standard floating-point formats in Fig. 1c. A standard floating-point format contains four components: a sign bit, an exponent, a mantissa, and an exponent bias [31]. A common one used for ML is MinFloat (FP8) proposed by Sun et al. [52], as illustrated at the top of the figure. It has 8 bits overall, and the exponent bias in this format is set as a fixed constant of 7. We now introduce three MX formats. First, the Microscaling Integers (MXInt) format, also known as the Block floating-point (BFP) format [32], shares the exponent in a block. The shared exponent bounds the range of values in the block and works well for values with small typical variation between magnitudes of the components in a block. Second, the Block Minifloat (BMF) [24] format shares the exponent bias in a block. This representation achieves high precision and range simultaneously, albeit with a larger quantization error around the medium of its range compared to the standard floating-point format. It is potentially suitable for values in a multi-modal distribution, efficiently representing values close to a peak within a block. Finally, the Block Logarithm (BL) format [43] strips out the mantissa and shares the exponent bias, resulting in values that are always powers of two. This contrasts with MXInt and is suitable for values with large dynamic ranges.

Table 1 shows the quantization results using different arithmetic formats for LLaMA on Wikitext2. To ensure fairness, all the arithmetic types have an average bitwidth of 8 bits. We evaluate them using three metrics, perplexity, memory density, and arithmetic density. The memory and arithmetic densities represent the normalized average values per bit and normalized average area per arithmetic operation compared to FP32 [14]. Both memory and arithmetic densities are derived from our post-routing hardware GEMM implementation using these arithmetic types. From the table, we made following observations. First, traditional 8-bit fixedpoint (Int8) quantization achieves decent memory and arithmetic density but suffers from a significant increase in perplexity. Second, FP8 achieves the best hardware efficiency, with an increase in perplexity. Finally, MX formats, such as MXInt, have competitive memory density and arithmetic density, and can preserve low perplexity. This motivates us to explore custom MX formats for LLM quantization and further improve hardware area efficiency with minimal precision loss.

What is the most efficient data format and its precision for quantizing an LLM? Given an LLM, the proposed compiler, MASE, automatically finds a mixed-precision MX quantization solution and



(b) Quantized model in MASE IR.

(c) A graph view of operation and value attributes of the reorder and linear operation in the model. Here we highlight software-specific and hardware-specific attributes.

Figure 2: A toy model in MASE IR after quantization and hardware parallelism.

maps it into an efficient dataflow accelerator for inference. In the rest of the paper, we show how to exploit our proposed abstraction MASE IR for efficient design exploration using MX formats.

3 MASE INTERMEDIATE REPRESENTATION

Existing hardware compilers for ML accelerators suffer from two main problems. First, they focus on operations with fixed-point and floating-point formats. Designers need to manually re-implement the whole design from scratch when mapping models with custom data formats. Second, the hardware-aware IR in those hardware compilers, such as LLVM [36] and MLIR [37], do not preserve backforward propagation functions. This means that a software model lowered into such an IR can no longer be further trained. When training is required, designers need to restart from a state in the software flow and may abandon all applied hardware optimizations if an additional software optimization is applied. In order to overcome these two challenges, we propose MASE IR, a hardware-aware and 'trainable' software intermediate representation that describes both a software model and the corresponding hardware accelerator architecture. MASE IR provides an efficient interface for users to integrate custom data formats for hardware exploration, and also keeps backward propagation functions so that the model can be trained or fine-tuned in hardware optimization cycles.

Like most IR languages, the syntax of MASE IR follows the traditional static single-assignment form [11]. The SSA form already provides a dataflow-like representation of a model. This enables direct translation into a dataflow hardware representation where each software module is mapped into a hardware component as illustrated in Fig. 1d and connected to other components using handshake interface. An operation in MASE IR contains a set of components, arguments, results, parameters and attributes:

result: type = operator(arg: type, ...) [param: type, ...] {attr, ...}

MASE IR is general for representing any ML model to explore optimizations with custom data formats. For example, Fig. 2a illustrates a toy model that contains a Linear operation followed a ReLU function. The input tensor is flattened before being sent to the linear operation. Fig. 2b represents the quantized toy model instance in Table 2: Key MASE passes used in this work. MASE contains 44 analysis and optimization passes. All these passes target different granularities varying from the model level to the bit level. These passes are general and type independent, which opens up opportunities for optimizing new data formats. Here we highlight software-specific and hardware-specific components.

Names	Descriptions
profile	Profile variation of values for a given dataset, used to define the quantization search space.
quantize	Quantize a given model based on an input configuration, used to perform tensor-level mixed-precision quantization for a given data format.
parallelize	Exploit resource-constrained hardware parallelism based on a given hardware target, leading to a hardware design with high area efficiency.
evaluate	Evaluate the hardware design based on a given expression of cost function, taking both model accuracy and area efficiency as arguments.
search	Orchestrate existing search algorithms, such as random search and Tree-structured Parzen Estimator (TPE), to ex- plore quantization search.
emit	Translate a co-design in MASE IR into a dataflow hardware accelerator in SystemVerilog.

MASE IR. All the tensors in the model including both activations and parameters are quantized in custom-precision MXInt formats for smaller bitwidths. For example, a type of MXint((16, 2), 8, 7) means that the elements of the tensor shares an 8-bit exponent for every block of size 16 by 2, and every element has a 7-bit mantissa. A model in MASE IR also carries detailed hardware design attributes for parallelism exploration, as illustrated in Fig. 2c. The operation attributes specify which hardware IP block is used for exploration and its estimated circuit area. The value attributes describe each dataflow edge in Fig. 1d. As illustrated in Fig. 2c, these include the shape of streaming tiles, the streaming order, hardware data interface, and estimated throughput. This allows the model optimizer to interface existing tools to exploit hardware parallelism.



Figure 3: Orchestration of existing tools for new data formats exploration. Given both software and hardware specifications for a new data format, MASE automatically explores resource-constrained quantization search for a given LLM.

3.1 Passes for Quantization Search and Dataflow Optimization

MASE contains a large set of passes targeting analysis and optimizations at different granularities ranging from the model level to the bit level. To minimize additional development for the new format, all MASE passes are type-independent, so that they can be orchestrated for optimizations of any data format. A set of key passes used in this work are listed in Table 2. The left of Fig. 3 provides an example of quantization search flow in MASE IR. In this example, the toy model in Fig. 2a is translated into MASE IR from PyTorch. The MASE front-end automatically performs model analysis and initializes software attributes when constructing MASE IR, such as tensor shapes and initial data types. For complex models, implicit dataflow-specific operations may also be inserted, such as 'reorder' in Fig. 1d. For simplicity, here we focus only on the toy model. (1) The model is quantized by the quantize pass using a set of user-defined precisions, which supports both post-training quantization (PTQ) and quantization-aware training (QAT). For this example, the model is quantized into MXInt format at the tensor level. The parameters have a lower bitwidth compared to activations because they are less sensitive. (2) Then the parallelize pass exploits hardware parallelism for the quantized model. Given a hardware resource budget, it automatically explores the most efficient stream tile sizes for each layer, leading to an optimized overall throughput. The hardware mapping solution contains several hardware design parameters illustrated in Fig. 2c. (3) Since MASE IR contains both software and hardware design parameters, the accuracy of the model and the area efficiency of the final hardware can be estimated by program analysis at the source level using the evaluate pass. These design constraints form a hardware-aware cost function, which could guide exploration of both following software and hardware optimizations. ④ Guided by the cost function, the search pass iterates quantization and hardware parallelism to find an efficient mixed-precision quantization for a given model. It orchestrates existing search algorithms, such as TPE (Tree-structured

Parzen Estimator) [45], for efficient exploration with custom data formats. (5) After a given number of iterations, the model is then mapped into a dataflow hardware design in SystemVerilog. The emit pass performs direct translation without any program analysis because all the hardware design parameters of the model are accessible in MASE IR.

3.2 Pass Orchestration for Custom Data Formats

MASE is general and allows for seamless integration of new data formats for resource-constrained quantization. The right of Fig. 3 shows our optimization orchestration flow, where users only need to add the blue part of the code for a new data format. There are two components to be added for a new data format, software emulators and hardware components. First, software emulators specify how to quantize and dequantize the value between the given format and floating-point numbers. For each operation, the input data is first quantized into a given input precision. Then the same existing operation in PyTorch is orchestrated to carry out the calculation in floating-point numbers. The results in floating-point numbers are further quantized to a given output precision. A main advantage of such an approach is that MASE can orchestrate existing floating-point operations to emulate operations with custom data formats without re-defining all the operations from scratch. The software emulators provide a fast evaluation of model performance in accuracy, which guides further software optimizations, such as the iterative quantization search.

Second, designs for such hardware operators can be diverse, making it challenging for existing tools to estimate hardware results. To restrict the design space, the hardware designs of operators with new data formats are required for architecture exploration and evaluation. Each component is provided as a Verilog template of a dataflow component with a set of parameters for data parallelism, such as input stream tile sizes. For example, the right of Fig. 3 illustrates a high-level view of a dot product operation with four data formats illustrated in Fig. 1c. The light purple blocks represent fixed-point or logic operators which have small area, and the dark



Figure 4: Evaluation of search algorithms for OPT125M on sst2. MASE orchestrates existing search algorithms to explore resource-constrained quantization with mixed-precision MX-Int formats. The cost function is shown on the y label (described in Section 4. acc = accuracy, b = average bitwidth. k is a hyperparameter to normalize costs. We observed that TPE is the most efficient search algorithm for MXInt quantization.

purple blocks represent floating-point operators which have large area. Compared to the traditional floating-point operator on the top left, the *MXInt* operator saves significant area by reusing the results of the shared exponent in the block because one of the main area costs of a floating-point operator is the dynamic shift hardware unit [10]; the *BMF* operator, on the other hand, requires more circuit area to calculate values with the shared exponent bias, while expanding the dynamic range of each element; the *BL* operator saves area from the BMF operator by stripping out operators for the mantissas, leading to a low precision in a small range.

With the provided hardware templates, MASE automatically explores hardware designs by sweeping the parallelism parameters. This is a one-off process, and a regression model enables MASE to estimate the overall throughput and total circuit area at the source level. MASE orchestrates existing optimization algorithms for dataflow architecture exploration and uses the regression model to guide the process. This leads to an efficient co-design with both high area efficiency and accuracy. The provided Verilog templates are also used for final hardware generation. Because all hardware components are implemented in a dataflow architecture, they can be directly integrated into the design by connecting the handshake interface. *The MX software emulators and hardware components will be open source as well as the MASE tool.*

3.3 Scalability Analysis

Optimization orchestration enables users to explore a range of new data formats at scale. This minimizes development time and effort and allows users to focus on exploring efficient data formats using advanced algorithms. For example, Fig. 4 evaluates four well-known search algorithms orchestrated by MASE for resource-constrained mixed-precision MXInt quantization on OPT-125M, Random Search, Non-dominated Sorting Genetic Algorithm II (NSGA-II) [16], Quasi-Monte Carlo (QMC) sequences [3],

Table 3: Line-of-Code comparison for OPT. MASE IR provides an efficient representation of an ML model at the module level and enables fast compilation time compared to existing hardware design IR, such as MLIR affine. DAG = code in directed acyclic graph.

Models	MLIR affine DAG Size	Codegen Time	MASE IR DAG size	Codegen Time	Code size ×
OPT-125M	1.9M	1 week	61	23s	31.1k
OPT-350M	1.7M	2 weeks	86	63s	19.7k
OPT-1.3B	1.7M	>4 weeks	86	112s	19.7k
OPT-2.7B	1.9M	>4 weeks	101	217s	18.8k
OPT-6.7B	2.3M	>4 weeks	101	467s	22.8k

and Tree-structured Parzen Estimator (TPE) [2]. Random Search is an elementary method that involves exploring the solution space by generating random configurations. The NSGA-II method is a multiobjective optimization algorithm that operates on the principles of evolutionary algorithms, wherein a population of candidate solutions undergoes a process of evolution through selection, crossover, and mutation operators. The QMC method is a class of numerical integration techniques used for high-dimensional problems where the use of traditional Monte Carlo (MC) methods would be computationally infeasible. The TPE method is a Bayesian optimization algorithm that models the dependency between hyperparameters to efficiently discover the promising areas of the hyperparameter search space.

In comparison, random search serves as a straightforward baseline but has the minimum change between the starting design point and the final design point. This is due to the lack of a guided search strategy. NSGA-II has a slightly larger change and leads to a better design, efficiently trading off between the accuracy and memory size. The QMC method has the fastest search speed but results in a sub-optimal design. TPE, although it has the worst starting point, can be effectively improved over time and results in the best design among all the algorithms. The average search times for all these algorithms are close. This suggests that the TPE is the most efficient algorithm to search for mixed-precision MXInt quantization, so we use the TPE algorithm in our experiments.

MASE IR also provides a compact representation for exploration of large models. It efficiently expresses the dataflow architecture for a large model up to billions of parameters and achieves significant scalability improvements in compilation time compared to existing hardware IRs. Here we compare MASE IR with the MILR affine dialect [37], a commonly used hardware compilers [7, 65, 73]. Table 3 compares the code size of MLIR and MASE IR in directed acyclic graph (DAG) size. In the table, we observe that MASE IR has shown a significantly smaller code size than MLIR affine, because it expresses operations at the module level, hiding the instruction-level details from users. The detailed MLIR enables a finer-grained hardware optimization but the code size overhead causes the compilation time to increase exponentially. In MASE, the optimizations focus on the modules, where instruction-level optimizations are manually carried out in the Verilog templates and linked to the tunable parameters. This reduces the compilation complexity while preserving high hardware efficiency. In addition,

the hardware attributes in MASE IR also enables MASE to interface with these hardware compilers to explore instruction-level optimizations in MLIR by loading their generated hardware designs instead of Verilog templates for regression modeling in Fig. 3.

4 MIXED-PRECISION MXINT QUANTIZATION

We will now demonstrate the exploration of MX formats quantization using MASE. Insights derived from Table 1 indicate that among the evaluated MX formats, MXInt is better suited for quantizing the LLaMA model. Fig. 5 further verifies the same phenomenon across 10 different LLMs. To ensure fairness, every model is quantized to a given format with an average bitwidth of 8 bits, and mapped onto dataflow hardware using the same hardware optimizations. The bars represent the normalized hardware area efficiency of each design to the standard dataflow hardware implementation using 8-bit fixed point numbers (int8). Larger area efficiency means more efficient hardware design. The curves plot the difference in accuracy compared to the accuracy of the model in FP32. A larger accuracy difference means higher accuracy.

MXInt is the most amenable for quantizing LLMs. In general, MX formats require more complex circuit design, leading to lower area efficiency compared to int8; however, their dynamic ranges lead to better accuracy. Among these MX formats, we observed that the MXInt format achieves both the best area efficiency and the best accuracy for most models.¹ This suggests that for most values in these LLMs, their elements in each tenor have small differences from their neighbor elements. We conclude that MXInt is more suitable for quantizing LLMs. In this section, we take MXInt for example, and illustrated our proposed mixed-precision MXInt quantization for LLMs.

No mixed-arithmetic but mixed-precision quantization. Another possibility is to mix arithmetic types as well as mixing precisions, however, the area overhead is large. These formats, such as MXInt and BL, have significant differences in both shared and local elements. The casting function between these formats requires complex dynamic shift operations to align their ranges before any further calculations. This would lead to significant circuit area compared to computing using a single arithmetic type. On the other hand, casting values in different precisions of the same format is more affordable in hardware. Here we take MXInt, for example. Casting mantissas only requires bit extension or truncation, similar to fixed-point numbers. The exponents may require dynamic shift, but the shift operation can be fully unrolled into logic wires at low cost because the bitwidth of mantissas is small. Therefore, mixed-precision MXInt quantization has a low area overhead in type casting between values.

4.1 Software Design Parameters

The quantization search for MXInt formats involves two sets of constraints, software and hardware. Here we show how to formalize the design parameters and restrict the search space for better search efficiency. Search efficiency entails finding a precise quantization solution with high accuracy and small circuit area using minimal number of trails.





Figure 5: Evaluation of three MX data formats for quantizing LLMs on sst2. The area efficiency results are plotted relative to int8 results (higher means better). The accuracy are represented as its difference with the accuracy using FP32 (higher means better). To ensure fairness, all the formats have a block size of 32 that contains an 8-bit shared component and 8-bit local components, leading to an average bitwidth of 8 bits. Overall, MXInt has shown both high area efficiency and high accuracy for LLM quantization.

For each parameter or activation value, its MXInt format is a 3-tuple, (B, e, m).

- B ∈ ℝ^N denotes the shape of the block, indicating how the exponent is shared among elements inside the block. A block usually has two dimensions, where N = 2;
- $e \in \mathbb{N}$ is the bitwidth of the shared exponent of each block; and
- $m \in \mathbb{N}$ is the bitwidth of the mantissa for each element.

The average bitwidth p of a value is the sum of the exponent bits per element, the mantissa bits and the sign bit:

$$p = \frac{e}{\Pi B} + m + 1 \tag{1}$$

For example, a value of MXint((16, 2), 8, 7) shown in Fig. 2b has an average bitwidth of 8.25. Assume that all blocks have two dimensions. We have the total search space S as follows:

S

$$=\mathbb{N}^{4v} \tag{2}$$

v is the total number of values in the model to be quantized. Each value has four parameters to explore for their precision. Such a search space is significantly huge in a large model that contains hundreds of values. We now show how to efficiently reduce the search space, thus improving search efficiency.

Use a unified block shape for all values to reduce the search space. A large block size allows an exponent to be shared by more elements, reducing the average bitwidth, and a small block extends the flexibility of element ranges due to relatively more localized scaling factors. Mixed block shapes may achieve finer quantization granularity for each value. However, casting between MXInt formats with different block shapes also requires complex circuits to denormalize and renormalize elements in different blocks. Using a unified block shape is beneficial for reducing quantization search and hardware design complexity. Prior work has shown that a block size of 32 for MXInt can achieve accuracy comparable to FP16 [14, 44]. Here we use a block shape of 16 by 2 for all MXInt formats.

Use a fixed bitwidth for all shared exponents. A small exponent leads to a small average bitwidth. However, its effect is negligible when the block size is large. For example, reducing by a bit only causes a reduction of $\frac{1}{32}$ in the average bitwidth for MX-Int formats with a block size of 32. Searching for small exponent bits exponentially expands the search space with nearly no benefit. Instead, we use an 8-bit exponent for all MXInt formats. The design parameters now only have variable mantissa bits, leading to a reduced search space *S*':

$$S' = \mathbb{N}^{v} \tag{3}$$

The mantissa bitwidths are essential for quantizing LLMs because the value differences are small.

MXInt formats have a smaller search space than fixedpoint numbers. Our formalization and analysis of MXInt quantization significantly reduce the search space. Compared to mixedprecision fixed-point search, which searches for both total bitwidth and fraction bitwidth for each value (search space of \mathbb{N}^{2v}), MX-Int quantization searches for mantissa bitwidth of each element, leading to a smaller search space.

4.2 Hardware Design Parameters

Hardware optimization techniques for dataflow accelerators have been widely studied in existing hardware compilers [21, 56, 57, 65]. Dataflow hardware optimization techniques typically involve two levels of parallelism.

Data Parallelism and Pipelining. The streaming tile of each value needs to be efficiently sized. A larger tile exploits more opportunities for spatial parallelism in hardware operators, which also take more hardware resources. The total hardware resources must be efficiently shared among these hardware operators to achieve high overall throughput. For example, different operators may compute at different throughputs because of different hardware behaviors. This means that a set of tile sizes need to be determined for balanced throughput between operators.

Memory Allocation. Fisrt, most parameter sizes of an LLM are large, taking large memory sizes. These data need to be efficiently allocated either on fast on-chip memory or large off-chip memory. An efficient memory allocation solution must be determined to maximize the efficient utilization of hardware resources and high throughput. Second, the data dependency between operators may cause pipeline stalls, affecting overall throughput. Buffers should be inserted between operators to resolve pipeline stalls to improve throughput.

These design considerations have been widely studied in dataflow hardware architectures for ML inference. Related works [50, 66, 72, 74] propose efficient algorithms to automatically determine an efficient dataflow hardware design, and these can be orchestrated by MASE for efficient hardware exploration. In this work, our scope focuses on optimization orchestration instead of algorithm efficiency. We integrate these hardware design considerations into the same TPE algorithm that runs the quantization search for resourceconstrained quantization. The circuit area is obtained from the regression model of hardware operators, and the overall throughput is the minimum throughput among all hardware operators estimated from the regression model.

4.3 Resource-Constrained Mixed-Precision Search

Adding hardware design parameters into the quantization search enables efficient software and hardware co-design. The search objective is as follows.

$$bb jective : \max(acc + \frac{k}{b} + k'\theta + \frac{k''}{A})$$
 (4)

acc is the model accuracy, *b* is the average bitwidth of the model, θ is estimated overall throughput, and *A* is the estimated total circuit area. *k*, *k'*, and *k''* are hyperparameters that normalize these design constraints.

5 EXPERIMENTS

We evaluated MASE on ten well-known LLMs from three families, including BERT [19], OPT [71] and LLaMA (including Vicuna and Alpaca) [8, 42, 54]. All of them are obtained directly from HuggingFace [30]. We evaluated the accuracy after mixed-precision MXInt quantization on six downstream tasks, including boolq [9], mnli [60], qnli [47], qqp [58], rte [12], and sst2 [51]. We evaluate the model accuracy following the same approach proposed by Zhang *et al.* [71] and Brown *et al.* [5]. We use Alveo U250 FP-GAs as the target platform for the evaluation of dataflow hardware design, and the version of the Xilinx software used is 2023.1. The throughput results are obtained from on-board measurements. The area and power results were obtained from the Post Place & Route report in Vivado.

In this section, we compare the accuracy and area efficiency of our mixed-precision MXInt (**MP MXInt**) approach with other metods. Second, we evaluate the effectiveness of our quantization on accuracy and average bitwidths for different sizes of OPT on six downstream tasks. Finally, we compare our mixed-precision approach with uniform-precision MXInt, and provide insights for ASIC accelerator designs.

5.1 Comparison with other quantization approaches

Here we compared the quality of our co-design with a few baselines. Fig. 7 shows the area efficiency of the dataflow hardware designs and model accuracy using different approach. **int8** means quantization using 8-bit fixed-point numbers. **MP int** means mixedprecision quantization using fixed-point numbers. **MP MXInt** means mixed-precision quantization using MXInt formats. Compared to MP MXInt, **MP MXInt (SW-only)** does not include hardware metrics for quantization search and uses the search objective shown in Fig. 4. **MXInt8** means quantization using the MXInt with 8-bit mantissas.

Compared with int8 and MXInt8 (in Fig. 5). The overhead in area efficiency of MP MXInt has significantly reduced compared to MXInt8 in Fig. 5. A major reason is the average bitwidth of MXInt mantissas has reduced to 4 bits thanks to the mixed-precision search. *The bitwidth reduction significantly reduces the circuit area for MXInt*



Figure 6: Evaluation of performance in accuracy for OPT across five model sizes and six datasets. MASE IR supports training in the hardware exploration loops, enabling resource-constrained quantization-aware training. For small models, all approaches applied quantization-aware training (QAT); and for large models, all approaches applied post-training quantization (PTQ).



Figure 7: Evaluation of MXInt data formats for quantizing LLMs on sst2. The area efficiency results are plotted relative to int8 (higher means better). The accuracy are represented as its difference with the accuracy using FP32 (higher means better).

while preserving the throughput, this leads to on average $1.31 \times$ area efficiency improvement. On average, MP MXInt has achieved similar area efficiency to int8. Also, the loss in accuracy caused by

bitwidth reduction is negligible, where both MP MXInt and MXInt8 achieve similar accuracy compared to FP32. This demonstrates that *our mixed-precision quantization effectively halves the average bitwidth at no accuracy loss.*

Compared with MP int. Prior work [17, 34, 46, 68] has observed that mixed-precision quantization using fixed-point numbers can lead to efficient hardware designs with high accuracy. In our experiments, we apply fine-grained mixed-precision quantization at the tensor level for both MP int and MP MXInt. Although MP int has achieved higher area efficiency compared to int8, its accuracy loss regarding the accuracy in FP32 is significant, making MP int infeasible. This is due to the absence of dynamic ranges in fixed-point numbers, leading to significant quantization errors in deeper layers, as illustrated in Fig. 1a. Our approach, MP MXInt, preserves high accuracy with an area efficiency overhead. *The area efficiency difference between MP MXInt and MP int closely mirrors that between int8 and MXInt8.*

Compared with MP MXInt (SW-only). A key novelty of MASE is adding hardware design metrics to quantization search, potentially leading to an efficient software and hardware co-design. Here we compare the same quantization search without hardware metrics with the MASE approach. On average, MP MXInt achieves



Figure 8: The energy efficiency of MP MXInt sits between MXInt4 and MXInt6. MP MXInt excels in accuracy and outperforms MXInt6 by 1% and MXInt4 by 8% respectively on average when evaluated on the sst2 dataset.

1.11× area efficiency of MP MXInt (SW-only). Although both approaches have achieved designs with high accuracy, *adding hardware metrics can guide the quantization search process towards a more area-efficient hardware design.*

5.2 Evaluation across model sizes and downstream tasks

Taking OPT for example, we demonstrate that our approach is broadly applicable across various model sizes and tasks as shown in Fig. 6. Different tasks share similar dataflow hardware designs, thus we focus on model accuracy and average bitwidth. MASE IR supports training concurrently with hardware exploration in the quantization search process. For smaller models, QAT progressively fine-tunes the model during the quantization process, achieving high accuracy; and for large models, PTQ is applied instead. Overall, Fig. 6 agrees with the previous observations. Individual discrepancies are caused by quantization noise.

MP MXInt achieves smaller average bitwidths than MP int. Over all the data points, MP MXInt has smaller average bitwidths than MP int by 0.5 bit, leading to an overhead of 10%. This overhead is due to the absence of dynamic ranges in fixed-point numbers, and more bits are required to cover the data range. Even with a larger bitwidth, MP int still fails to meet the same accuracy as MP MXInt. This indicates that the actual overhead may be larger when they have the same accuracy.

5.3 Insights for designing future ASIC accelerators

MASE exploits mixed-precision quantization at the tensor level to achieve high accuracy and area efficiency, leading to model-specific quantization. In applications where an accelerator may run inferences across multiple models, a more coarse-grained quantization may be amenable. Fig. 8 compares MP MXInt with another extreme of MXInt quantization that uniformly applies the same mantissa bits across all tensors. **MXInt6** means quantization using the MXInt format with 6-bit mantissas. Table 4: Runtime breakdown of the proposed toolflow, where the reported results are averaged across 10 LLMs. At the search stage, 64 trials are explored for each model.

Stage	Pass name	Time	
Pre-process	front-end profile	12s 97s	
Search (single trial)	quantize quantize (fine-tune) parallelize evaluate	5.3s 3201s 21 mins 376s	
Post-process	emit synthesize	153s 14.3 hours	

Trade-off between model-specific quantization and design quality remains challenging for MX formats. We evaluate the energy efficiency of the dataflow hardware accelerators, where MP MXInt sits between MXInt4 and MXInt6 due to its on average 4-bit mantissas. An interesting observation is that despite using 2 bits fewer on average, MP MXInt can still achieve better accuracy than MXInt6. This shows that *model-specific quantization can further push hardware efficiency significantly with no accuracy loss.* This provides insights to future accelerator design, where a trade-off needs to be explored between the granularity of model quantization and the generality of hardware designs. Such a design problem is application-specific and out of the scope of this work. However, MASE serves as a general open-source compiler and provide a platform for designers to explore potential ASIC accelerator architectures utilizing MX formats for domain-specific problems,

5.4 Optimization Compile Time

Table 4 illustrates the runtime of MASE passes. Both the pre-process and the post-process are run once for each model in the flow, and the search process is iteratively called for a given number of trials. The front-end of MASE pre-processes the model representation when parsing from PyTorch. The search time for each step is relatively fast compared to the synthesize time, where *our hardware evaluation model saves significant search time by source-level hardware design analysis and avoids repeatedly calling downstream synthesis tools.*

6 RELATED WORK

In this section, we first revisit related work in quantization using block arithmetic. Then we compare MASE and MASE IR with existing compilers and IRs. Finally, we review related work on LLM accelerator designs.

6.1 Block Arithmetic-based Quantization

Sharing certain components for a block of values has been widely recognized as the state-of-the-art technique for quantizing Convolutional Neural Networks (CNNs) [39, 70]. Further explorations within this line of research have investigated grouping numbers at various granularities, including layer-wise [61], channel-wise [35], and vector-wise quantization [13]. In addition, many block floating-point variants [13, 14, 28] have been proposed, with the core idea of grouping values into multiple blocks, and elements within each

block sharing common digits. Moreover, adjusting block sizes and mantissa bitwidths across layers provides finer quantization.

There are two closest pieces of work. [14] proposes an approach of MXInt quantization using the same precision, while we exploit mixed-precision MXInt quantization to further push the hardware efficiency on dataflow accelerators. [15] proposes multi-level MX formats, also known as Microscaling floating-point (MXFP), where the shared component can be non-integers, while we only restrict our scope on sharing integer components as illustrated in Fig. 1c. Exploring the hardware efficiency of MXFP operators involves different challenges in both quantization search and hardware realization, which will be our future work.

6.2 ML Dataflow Compilers and IRs

Most dataflow compilers for ML inference focus on DNNs. Xilinx FINN [56], HLS4ML [21], DNNBuilder [72], FPGAConvNet [57], and HIDA [66] have shown promising results in generating efficient dataflow accelerators. However, they only support hardware mapping from quantized models using fixed-point numbers, while **MASE is the first dataflow compiler that supports MX formats.** MASE comes with an open-source MX hardware operator library, and can automatically generate dataflow hardware accelerators using MX formats. Optimizations for dataflow architectures are actively studied [50, 74], and these techniques can be orchestrated into MASE for systematic exploration with MX formats.

Most compilers for ML training and inference use software IRs, such as TorchScript [18], ONNX [1] and FX Torch [48]. These IRs are often target-independent. Users need to manually add hardware intrinsic to explore target-specific optimizations, while MASE IR targets dataflow hardware architecture with built-in hardware intrinsics. TVM [6] has similar IRs for GPU-specific optimizations, while MASE focuses on dataflow architectures. Languages implemented in MLIR [37] or LLVM IR [36] are commonly used in hardware compilers but do not support training because the back propagation functions are lost when the model is lowered from PyTorch, while MASE IR is target-specific and keeps the model trainable for optimizations such as QAT.

6.3 Quantized LLM-related Accelerators

Quantization for efficient accelerator designs has been widely studied, especially using fixed-point numbers [17, 20, 25, 62, 64]. Prior work focuses on custom hardware architecture for efficient inference [22, 26, 27, 29, 33, 38, 41]. GOBO [67], EdgeBERT [53] exploits software and hardware co-designs for accelerating transformers. FACT [46] and FlightLLM [68] exploits mixed-precision quantization using fixed-point numbers for linear layers. They only focus on quantization using fixed-point numbers, and **MASE is the first approach to designing LLM accelerators using mixed-precision MX quantization**.

7 CONCLUSION

LLM inference today suffers from a rapid increase of the number of parameters, leading to both memory and computing challenges. While most existing methods address these challenges by quantizing LLMs into low-precision data formats, our work highlights the "scaling offsets" observed in such quantization. We propose a novel dataflow compiler named MASE to explore MX formats for efficient LLM inference on dataflow hardware accelerators. **MASE is the first hardware compiler to exploit hardware-aware quantization using mixed-precision MX formats.** Another contribution of MASE is that it comes with a set of open-source MX hardware operator IPs and can directly map a quantized model using MX formats into efficient dataflow hardware accelerator.

We also propose MASE IR, an efficient software and hardware co-design IR, and show how to orchestrate existing optimizations for new data formats in MASE IR. MASE IR provides an open platform for designers to explore new data formats for ML hardware accelerators, minimizing their development effort and time. By exploiting mixed-precision MXInt quantization on LLMs, we verified the great potential in MXInt formats for hardware-efficient LLM inference acceleration. Experimental data reveal that a hardware design employing mixed-precision MXInt has achieved similar area efficiency with int8 implementation with 24% accuracy improvements. Our results provide a performance upper bound reference for future MXInt-based accelerator designs, including ASIC accelerators.

Future ML accelerators should exploit mixed-precision MXInt formats. Our proposed MASE compiler is the first attempt to enable exploration of future accelerators. Our future work will involve several directions. First, we plan to improve our analysis and optimization passes for deeper integration of complex MX formats, such as MXFP [15]. This would expand the existing MX hardware design space. Second, we plan to extend MASE to support other hardware architectures, such as systolic arrays, and explore MX formats across different granularities. This might be further extended to explore the possibility of using MASE to model and simulate ASIC MX accelerators. Finally, we will evaluate MASE on other data formats to understand the practical limitations of the approach.

REFERENCES

- Junjie Bai, Fang Lu, Ke Zhang, et al. 2019. Onnx: Open neural network exchange. GitHub repository (2019), 54.
- [2] James Bergstra, Rémi Bardenet, Yoshua Bengio, and Balázs Kégl. 2011. Algorithms for hyper-parameter optimization. Advances in neural information processing systems 24 (2011).
- [3] James Bergstra and Yoshua Bengio. 2012. Random search for hyper-parameter optimization. *Journal of machine learning research* 13, 2 (2012).
- [4] Sid Black, Leo Gao, Phil Wang, Connor Leahy, and Stella Biderman. 2021. GPT-Neo: Large Scale Autoregressive Language Modeling with Mesh-Tensorflow. https://doi.org/10.5281/zenodo.5297715 If you use this software, please cite it using these metadata.
- [5] Tom Brown, Benjamin Mann, Nick Ryder, Melanie Subbiah, Jared D Kaplan, Prafulla Dhariwal, Arvind Neelakantan, Pranav Shyam, Girish Sastry, Amanda Askell, et al. 2020. Language models are few-shot learners. Advances in neural information processing systems 33 (2020), 1877–1901.
- [6] Tianqi Chen, Thierry Moreau, Ziheng Jiang, Lianmin Zheng, Eddie Yan, Haichen Shen, Meghan Cowan, Leyuan Wang, Yuwei Hu, Luis Ceze, et al. 2018. {TVM}: An automated {End-to-End} optimizing compiler for deep learning. In 13th USENIX Symposium on Operating Systems Design and Implementation (OSDI 18). 578–594.
- [7] Jianyi Cheng, Samuel Coward, Lorenzo Chelini, Rafael Barbalho, and Theo Drane. 2023. SEER: Super-Optimization Explorer for HLS using E-graph Rewriting with MLIR. arXiv preprint arXiv:2308.07654 (2023).
- [8] Wei-Lin Chiang, Zhuohan Li, Zi Lin, Ying Sheng, Zhanghao Wu, Hao Zhang, Lianmin Zheng, Siyuan Zhuang, Yonghao Zhuang, Joseph E Gonzalez, et al. 2023. Vicuna: An open-source chatbot impressing gpt-4 with 90%* chatgpt quality. See https://vicuna. lmsys. org (accessed 14 April 2023) (2023).
- [9] Christopher Clark, Kenton Lee, Ming-Wei Chang, Tom Kwiatkowski, Michael Collins, and Kristina Toutanova. 2019. BoolQ: Exploring the surprising difficulty of natural yes/no questions. arXiv preprint arXiv:1905.10044 (2019).
- [10] Samuel Coward, George A Constantinides, and Theo Drane. 2023. Automating constraint-aware datapath optimization using e-graphs. In 2023 60th ACM/IEEE Design Automation Conference (DAC). IEEE, 1-6.
- [11] Ron Cytron, Jeanne Ferrante, Barry K Rosen, Mark N Wegman, and F Kenneth Zadeck. 1991. Efficiently computing static single assignment form and the control dependence graph. ACM Transactions on Programming Languages and Systems (TOPLAS) 13, 4 (1991), 451–490.
- [12] Ido Dagan, Oren Glickman, and Bernardo Magnini. 2005. The pascal recognising textual entailment challenge. In *Machine learning challenges workshop*. Springer, 177–190.
- [13] Steve Dai, Rangha Venkatesan, Mark Ren, Brian Zimmer, William Dally, and Brucek Khailany. 2021. Vs-quant: Per-vector scaled quantization for accurate low-precision neural network inference. *Proceedings of Machine Learning and Systems* 3 (2021), 873–884.
- [14] Bita Darvish Rouhani, Daniel Lo, Ritchie Zhao, Ming Liu, Jeremy Fowers, Kalin Ovtcharov, Anna Vinogradsky, Sarah Massengill, Lita Yang, Ray Bittner, et al. 2020. Pushing the limits of narrow precision inferencing at cloud scale with microsoft floating point. Advances in neural information processing systems 33 (2020), 10271–10281.
- [15] Bita Darvish Rouhani, Ritchie Zhao, Venmugil Elango, Rasoul Shafipour, Mathew Hall, Maral Mesmakhosroshahi, Ankit More, Levi Melnick, Maximilian Golub, Girish Varatkar, et al. 2023. With Shared Microexponents, A Little Shifting Goes a Long Way. In Proceedings of the 50th Annual International Symposium on Computer Architecture. 1–13.
- [16] Kalyanmoy Deb, Amrit Pratap, Sameer Agarwal, and TAMT Meyarivan. 2002. A fast and elitist multiobjective genetic algorithm: NSGA-II. *IEEE transactions on* evolutionary computation 6, 2 (2002), 182–197.
- [17] Tim Dettmers, Mike Lewis, Younes Belkada, and Luke Zettlemoyer. 2022. Llm. int8 (): 8-bit matrix multiplication for transformers at scale. arXiv preprint arXiv:2208.07339 (2022).
- [18] Zachary DeVito. 2022. Torchscript: Optimized execution of pytorch programs. *Retrieved January* (2022).
- [19] Jacob Devlin, Ming-Wei Chang, Kenton Lee, and Kristina Toutanova. 2019. BERT: Pre-training of Deep Bidirectional Transformers for Language Understanding. arXiv:1810.04805 [cs.CL]
- [20] Zhen Dong, Zhewei Yao, Amir Gholami, Michael W Mahoney, and Kurt Keutzer. 2019. Hawq: Hessian aware quantization of neural networks with mixedprecision. In Proceedings of the IEEE/CVF International Conference on Computer Vision. 293–302.
- [21] Farah Fahim, Benjamin Hawks, Christian Herwig, James Hirschauer, Sergo Jindariani, Nhan Tran, Luca P Carloni, Giuseppe Di Guglielmo, Philip Harris, Jeffrey Krupa, et al. 2021. hls4ml: An open-source codesign workflow to empower scientific low-power machine learning devices. arXiv preprint arXiv:2103.05579 (2021).

- [22] Hongxiang Fan, Thomas Chau, Stylianos I Venieris, Royson Lee, Alexandros Kouris, Wayne Luk, Nicholas D Lane, and Mohamed S Abdelfattah. 2022. Adaptable butterfly accelerator for attention-based NNs via hardware and algorithm co-design. In 2022 55th IEEE/ACM International Symposium on Microarchitecture (MICRO). IEEE, 599–615.
- [23] Fangxiaoyu Feng, Yinfei Yang, Daniel Cer, Naveen Arivazhagan, and Wei Wang. 2020. Language-agnostic BERT sentence embedding. arXiv preprint arXiv:2007.01852 (2020).
- [24] Sean Fox, Seyedramin Rasoulinezhad, Julian Faraone, Philip Leong, et al. 2021. A block minifloat representation for training deep neural networks. In *International Conference on Learning Representations.*
- [25] Elias Frantar, Saleh Ashkboos, Torsten Hoefler, and Dan Alistarh. 2022. GPTQ: Accurate Post-Training Quantization for Generative Pre-trained Transformers. arXiv preprint arXiv:2210.17323 (2022).
- [26] Tae Jun Ham, Sung Jun Jung, Seonghak Kim, Young H Oh, Yeonhong Park, Yoonho Song, Jung-Hun Park, Sanghee Lee, Kyoung Park, Jae W Lee, et al. 2020. A³: Accelerating attention mechanisms in neural networks with approximation. In 2020 IEEE International Symposium on High Performance Computer Architecture (HPCA). IEEE, 328–341.
- [27] Tae Jun Ham, Yejin Lee, Seong Hoon Seo, Soosung Kim, Hyunji Choi, Sung Jun Jung, and Jae W Lee. 2021. ELSA: Hardware-software co-design for efficient, lightweight self-attention mechanism in neural networks. In 2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA). IEEE, 692–705.
- [28] Simla Burcu Harma, Canberk Sönmez, Babak Falsafi, Martin Jaggi, and Yunho Oh. 2022. Accuracy Boosters: Epoch-Driven Mixed-Mantissa Block Floating-Point for DNN Training. arXiv preprint arXiv:2211.10737 (2022).
- [29] Seongmin Hong, Seungjae Moon, Junsoo Kim, Sungjae Lee, Minsub Kim, Dongsoo Lee, and Joo-Young Kim. 2022. DFX: A low-latency multi-FPGA appliance for accelerating transformer-based text generation. In 2022 55th IEEE/ACM International Symposium on Microarchitecture (MICRO). IEEE, 616–630.
- [30] Hugging Face. 2023. https://huggingface.co/
- [31] William Kahan. 1996. IEEE standard 754 for binary floating-point arithmetic. Lecture Notes on the Status of IEEE 754, 94720-1776 (1996), 11.
- [32] Kari Kalliojarvi and Jaakko Astola. 1996. Roundoff errors in block-floating-point systems. IEEE transactions on signal processing 44, 4 (1996), 783–790.
- [33] Sheng-Chun Kao, Suvinay Subramanian, Gaurav Agrawal, Amir Yazdanbakhsh, and Tushar Krishna. 2023. FLAT: An Optimized Dataflow for Mitigating Attention Bottlenecks. In Proceedings of the 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2. 295–310.
- [34] Sehoon Kim, Coleman Hooper, Amir Gholami, Zhen Dong, Xiuyu Li, Sheng Shen, Michael W Mahoney, and Kurt Keutzer. 2023. Squeezellm: Dense-and-sparse quantization. arXiv preprint arXiv:2306.07629 (2023).
- [35] Raghuraman Krishnamoorthi. 2018. Quantizing deep convolutional networks for efficient inference: A whitepaper. arXiv preprint arXiv:1806.08342 (2018).
- [36] Chris Lattner and Vikram Adve. 2004. LLVM: A compilation framework for lifelong program analysis & transformation. In *International symposium on code* generation and optimization, 2004. CGO 2004. IEEE, 75–86.
- [37] Chris Lattner, Mehdi Amini, Uday Bondhugula, Albert Cohen, Andy Davis, Jacques Pienaar, River Riddle, Tatiana Shpeisman, Nicolas Vasilache, and Oleksandr Zinenko. 2021. MLIR: Scaling compiler infrastructure for domain specific computation. In 2021 IEEE/ACM International Symposium on Code Generation and Optimization (CGO). IEEE, 2–14.
- [38] Bingbing Li, Santosh Pandey, Haowen Fang, Yanjun Lyv, Ji Li, Jieyang Chen, Mimi Xie, Lipeng Wan, Hang Liu, and Caiwen Ding. 2020. Ftrans: energyefficient acceleration of transformers using fpga. In Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design. 175–180.
- [39] Xiaofan Lin, Cong Zhao, and Wei Pan. 2017. Towards Accurate Binary Convolutional Neural Network. arXiv:1711.11294 [cs.LG]
- [40] Jiachang Liu, Dinghan Shen, Yizhe Zhang, Bill Dolan, Lawrence Carin, and Weizhu Chen. 2021. What Makes Good In-Context Examples for GPT-3? arXiv preprint arXiv:2101.06804 (2021).
- [41] Liqiang Lu, Yicheng Jin, Hangrui Bi, Zizhang Luo, Peng Li, Tao Wang, and Yun Liang. 2021. Sanger: A co-design framework for enabling sparse attention using reconfigurable architecture. In MICRO-54: 54th Annual IEEE/ACM International Symposium on Microarchitecture. 977–991.
- [42] Xupeng Miao, Gabriele Oliaro, Zhihao Zhang, Xinhao Cheng, Zeyu Wang, Rae Ying Yee Wong, Zhuoming Chen, Daiyaan Arfeen, Reyna Abhyankar, and Zhihao Jia. 2023. SpecInfer: Accelerating Generative LLM Serving with Speculative Inference and Token Tree Verification. arXiv preprint arXiv:2305.09781 (2023).
- [43] Daisuke Miyashita, Edward H Lee, and Boris Murmann. 2016. Convolutional neural networks using logarithmic data representation. arXiv preprint arXiv:1603.01025 (2016).
- [44] OCP Microscaling Formats (MX) Specification. 2023. https://www.opencompute. org/documents/ocp-microscaling-formats-mx-v1-0-spec-final-pdf
- [45] Yoshihiko Ozaki, Yuki Tanigaki, Shuhei Watanabe, and Masaki Onishi. 2020. Multiobjective tree-structured parzen estimator for computationally expensive

optimization problems. In Proceedings of the 2020 genetic and evolutionary computation conference. 533–541.

- [46] Yubin Qin, Yang Wang, Dazheng Deng, Zhiren Zhao, Xiaolong Yang, Leibo Liu, Shaojun Wei, Yang Hu, and Shouyi Yin. 2023. FACT: FFN-attention Co-optimized transformer architecture with eager correlation prediction. In *Proceedings of the* 50th Annual International Symposium on Computer Architecture. 1–14.
- [47] Pranav Rajpurkar, Jian Zhang, Konstantin Lopyrev, and Percy Liang. 2016. Squad: 100,000+ questions for machine comprehension of text. arXiv preprint arXiv:1606.05250 (2016).
- [48] James Reed, Zachary DeVito, Horace He, Ansley Ussery, and Jason Ansel. 2022. torch. fx: Practical Program Capture and Transformation for Deep Learning in Python. Proceedings of Machine Learning and Systems 4 (2022), 638–651.
- [49] Bita Rouhani, Ritchie Zhao, Venmugil Elango, Rasoul Shafipour, Mathew Hall, Maral Mesmakhosroshahi, Ankit More, Levi Melnick, Maximilian Golub, Girish Varatkar, et al. 2023. Shared Microexponents: A Little Shifting Goes a Long Way. arXiv preprint arXiv:2302.08007 (2023).
- [50] Alexander C Rucker, Shiv Sundram, Coleman Smith, Matthew Vilim, Raghu Prabhakar, Fredrik Kjølstad, and Kunle Olukotun. 2024. Revet: A language and compiler for dataflow threads. In 2024 IEEE International Symposium on High-Performance Computer Architecture (HPCA). IEEE, 1–14.
- [51] Richard Socher, Alex Perelygin, Jean Wu, Jason Chuang, Christopher D Manning, Andrew Y Ng, and Christopher Potts. 2013. Recursive deep models for semantic compositionality over a sentiment treebank. In *Proceedings of the 2013 conference* on empirical methods in natural language processing. 1631–1642.
- [52] Xiao Sun, Jungwook Choi, Chia-Yu Chen, Naigang Wang, Swagath Venkataramani, Vijayalakshmi Viji Srinivasan, Xiaodong Cui, Wei Zhang, and Kailash Gopalakrishnan. 2019. Hybrid 8-bit floating point (HFP8) training and inference for deep neural networks. Advances in neural information processing systems 32 (2019).
- [53] Thierry Tambe, Coleman Hooper, Lillian Pentecost, Tianyu Jia, En-Yu Yang, Marco Donato, Victor Sanh, Paul Whatmough, Alexander M. Rush, David Brooks, and Gu-Yeon Wei. 2021. EdgeBERT: Sentence-Level Energy Optimizations for Latency-Aware Multi-Task NLP Inference. In MICRO-54: 54th Annual IEEE/ACM International Symposium on Microarchitecture (Virtual Event, Greece) (MICRO '21). Association for Computing Machinery, New York, NY, USA, 830–844. https: //doi.org/10.1145/3466752.3480095
- [54] Hugo Touvron, Thibaut Lavril, Gautier Izacard, Xavier Martinet, Marie-Anne Lachaux, Timothée Lacroix, Baptiste Rozière, Naman Goyal, Eric Hambro, Faisal Azhar, et al. 2023. Llama: Open and efficient foundation language models. arXiv preprint arXiv:2302.13971 (2023).
- [55] Hugo Touvron, Louis Martin, Kevin Stone, Peter Albert, Amjad Almahairi, Yasmine Babaei, Nikolay Bashlykov, Soumya Batra, Prajjwal Bhargava, Shruti Bhosale, et al. 2023. Llama 2: Open foundation and fine-tuned chat models. arXiv preprint arXiv:2307.09288 (2023).
- [56] Yaman Umuroglu, Nicholas J Fraser, Giulio Gambardella, Michaela Blott, Philip Leong, Magnus Jahre, and Kees Vissers. 2017. Finn: A framework for fast, scalable binarized neural network inference. In Proceedings of the 2017 ACM/SIGDA international symposium on field-programmable gate arrays. 65–74.
- [57] Stylianos I Venieris and Christos-Savvas Bouganis. 2016. fpgaConvNet: A framework for mapping convolutional neural networks on FPGAs. In 2016 IEEE 24th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM). IEEE, 40–47.
- [58] Alex Wang, Amanpreet Singh, Julian Michael, Felix Hill, Omer Levy, and Samuel R. Bowman. 2019. GLUE: A Multi-Task Benchmark and Analysis Platform for Natural Language Understanding. In the Proceedings of ICLR.
- [59] Jason Wei, Yi Tay, Rishi Bommasani, Colin Raffel, Barret Zoph, Sebastian Borgeaud, Dani Yogatama, Maarten Bosma, Denny Zhou, Donald Metzler, et al. 2022. Emergent abilities of large language models. arXiv preprint arXiv:2206.07682 (2022).
- [60] Adina Williams, Nikita Nangia, and Samuel R Bowman. 2017. A broad-coverage challenge corpus for sentence understanding through inference. arXiv preprint arXiv:1704.05426 (2017).
- [61] Shuang Wu, Guoqi Li, Feng Chen, and Luping Shi. 2018. Training and inference with integers in deep neural networks. arXiv preprint arXiv:1802.04680 (2018).
- [62] Guangxuan Xiao, Ji Lin, Mickael Seznec, Julien Demouth, and Song Han. 2022. Smoothquant: Accurate and efficient post-training quantization for large language models. arXiv preprint arXiv:2211.10438 (2022).
- [63] Zekun Yang, Noa Garcia, Chenhui Chu, Mayu Otani, Yuta Nakashima, and Haruo Takemura. 2020. Bert representations for video question answering. In Proceedings of the IEEE/CVF Winter Conference on Applications of Computer Vision. 1556–1565.
- [64] Zhewei Yao, Reza Yazdani Aminabadi, Minjia Zhang, Xiaoxia Wu, Conglong Li, and Yuxiong He. 2022. ZeroQuant: Efficient and affordable post-training quantization for large-scale transformers. Advances in Neural Information Processing Systems 35 (2022), 27168–27183.
- [65] Hanchen Ye, Cong Hao, Jianyi Cheng, Hyunmin Jeong, Jack Huang, Stephen Neuendorffer, and Deming Chen. 2022. Scalehls: A new scalable high-level synthesis framework on multi-level intermediate representation. In 2022 IEEE

International Symposium on High-Performance Computer Architecture (HPCA). IEEE, 741–755.

- [66] Hanchen Ye, Hyegang Jun, and Deming Chen. 2023. HIDA: A Hierarchical Dataflow Compiler for High-Level Synthesis. arXiv preprint arXiv:2311.03379 (2023).
- [67] Ali Hadi Zadeh, Isak Edo, Omar Mohamed Awad, and Andreas Moshovos. 2020. Gobo: Quantizing attention-based nlp models for low latency and energy efficient inference. In 2020 53rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO). IEEE, 811–824.
- [68] Shulin Zeng, Jun Liu, Guohao Dai, Xinhao Yang, Tianyu Fu, Hongyi Wang, Wenheng Ma, Hanbo Sun, Shiyao Li, Zixiao Huang, et al. 2024. FlightLLM: Efficient Large Language Model Inference with a Complete Mapping Flow on FPGA. arXiv preprint arXiv:2401.03868 (2024).
- [69] Dan Zhang, Šafeen Huda, Ebrahim Songhori, Kartik Prabhu, Quoc Le, Anna Goldie, and Azalia Mirhoseini. 2022. A full-stack search technique for domain optimized deep learning accelerators. In Proceedings of the 27th ACM International Conference on Architectural Support for Programming Languages and Operating Systems. 27–42.
- [70] Dongqing Zhang, Jiaolong Yang, Dongqiangzi Ye, and Gang Hua. 2018. LQ-Nets: Learned Quantization for Highly Accurate and Compact Deep Neural Networks. arXiv:1807.10029 [cs.CV]
- [71] Susan Zhang, Stephen Roller, Naman Goyal, Mikel Artetxe, Moya Chen, Shuohui Chen, Christopher Dewan, Mona Diab, Xian Li, Xi Victoria Lin, et al. 2022. Opt: Open pre-trained transformer language models. arXiv preprint arXiv:2205.01068 (2022).
- [72] Xiaofan Zhang, Junsong Wang, Chao Zhu, Yonghua Lin, Jinjun Xiong, Wen-mei Hwu, and Deming Chen. 2018. DNNBuilder: An automated tool for building high-performance DNN hardware accelerators for FPGAs. In 2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). IEEE, 1–8.
- [73] Ruizhe Zhao, Jianyi Cheng, Wayne Luk, and George A Constantinides. 2022. Polsca: Polyhedral high-level synthesis with compiler transformations. In 2022 32nd International Conference on Field-Programmable Logic and Applications (FPL). IEEE, 235–242.
- [74] Tian Zhao, Alexander Rucker, and Kunle Olukotun. 2023. Sigma: Compiling einstein summations to locality-aware dataflow. In Proceedings of the 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2. 718–732.