Layered Control to Enable Large Scale SOA Switch Fabric

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Abstract A layered architecture is shown for construction and management of large-scale multi-stage SOA switch. The scheme is implemented in a 40Gb/s multi-stage SOA switch network. Output power of each packet is controlled to within 0.5dB.

Introduction
Increasingly sophisticated photonic integrated circuits with high numbers of active components such as multi-stage switch fabrics introduce complex control challenges. Studies on semiconductor optical amplifier (SOA) based switch fabrics have shown low penalty operation for high levels of cascading for wavelength multiplexed packets [1]. However, as the number of wavelengths, and therefore data capacity increases, the optimum operating regimes become more restrictive and fine tuning of the operating conditions for individual switches becomes critical.

On-the-fly electronic control of SOA gain has been proposed to reduce output power fluctuations for a specified input dynamic range by means of direct photocurrent detection in a preceding detector [2], a controlled gain-clamped SOA [3], and by means of narrow band voltage monitoring at the controlled SOA [4]. However, such schemes intrinsically require delays between the monitored signal and the data packet. This can lead to excessive guard-band times and or payload and header power level distortion. To manage the complexity of the control functions, we separate, 'layer', the control of individual device elements from control of the aggregate subsystem. The subsystem control is the interface to higher layers controlling network scheduling.

Multi-layer control
Four hierarchical control layers are used as in Fig 1; i) the central arbiter allocates transmission slots to the hosts, ii) the router determines the path and makes this information available to the switch controllers iii) the switch fabric controller determines the gain of the iv) individual the SOA gates. The SOA switch module makes the physical connection.

Routing operation is realised through two phases; calibration and operation. Information of the input power for each SOA module under all routing combinations is obtained during the pre-operational calibration phase. This involves the sequential testing of all paths connected to the device to be calibrated. The appropriate gating current for each routing combination is determined and stored in the switch controller. During the operational mode, the switch controller sets the SOA module with the appropriate switching current based on allocated routes and slots.

![Fig. 1. Experimental schematic showing layered control functionality.](image)

Test Bed
A switched optical test bed, as shown in fig. 1, with power equalisation module used at the second stage switch, is implemented to investigate the control scheme. To show the variations of transmission power between the different hosts in a network, three hosts each transmitting four 10Gb/s WDM channels from 1548.95µm to 1553.8µm region are used. Each host transmits decorrelated PRBS sequences of pattern length $2^{15}-1$. This sequence is selected due to constrains in the slot length. The PRBS generator is programmed to output either a continuous PRBS sequence or sequence with data packet lengths of 53µs interleaved a with guard band. The guard band is currently 5µs, limited by the response of the DAC in the SOA module. The guard band can be reduced to 20ns by use of an optimised DAC. Two partially populated, tree architecture 4x4 SOA switch modules with isolators and spliced splitters/combiners are used as the switch fabric. For the first stage of the switch fabric, three SOAs are used to allow adequate routing for the three connected hosts [5]. The second stage SOA switch, which routes the packets to the output, has the necessary components for modular realisation of power equalisation module. The SOA controller determines the optical input power through a 10:90 splitter. The 10% tapped optical input is
optically filtered with a bandwidth of 0.6nm, detected and digitised using a 12-bit ADC. The appropriate switching current for the SOA is correlated to the optical input power through the pre-calibrated look up table (LUT). Using the 12-bit DAC and current driver, the SOA controller switches the SOA with the bias current obtained from the LUT.

During the pre-operational calibration phase, the central arbiter triggers host A, B, C in turn to transmit a continuous PRBS sequence. The router exercises all possible routing paths by switching the optical signal into the second stage SOA in a round robin manner. The second stage SOA switch module samples the incoming optical power for each routing case and reports the appropriate switching current to the switch controller. The relation between the required switching current and the routing path is stored in the switch controller. In the operational mode, the arbiter instructs the hosts to transmit in packet format, and the router to route the packets to the test port. The switch controller provides the controlled SOA module with the appropriate switching currents based on the pre-allocated routes and slots.

Results

The waveforms on the left of Fig 2 show the input power into the first 4x4 switch fabric. The waveform on the right compares the output with and without power equalization. Per-packet power equalisation of 0dBm, with 0.5dB variation is achieved.

![Packet power equalization, equalized to 0dBm with 0.5dBm variation](image)

In order to test the automatic power equalisation, the input power for packet A is swept across a range from -16dBm to -4dBm, and the input powers of packet B and C are set to -18dBm and -12dBm respectively to stress the control scheme with a large power fluctuation across the input range of A. The SOA module equalises the power of each host to 0dBm. The BERT is trained to select packets only from host A for BER measurement. Wavelength 1548.95µm is selected using an AWG. The upper limit of input power is limited by hosts and the path power budget. The lower limit input power into the SOA is governed by the sensitivity of the power monitoring prior to the ADC. The BER curves are measured, and power penalties derived at 1dB intervals from -16dBm to -4dBm. Fig.3 shows the BER curves under automatic equalisation and are compared with the back-to-back measurement directly from host A. It can be seen that a BER penalty of less than 1.5dB is obtained for an input power range of greater than 10dB.

![Bit error rate (BER) as a function of receiver input power for power equalization scheme](image)

Discussion

Higher penalties are observed when packet A is at very low input powers owing to the high switching current required to equalise the output power to 0dBm. Penalties at high input powers are caused by SOA saturation.

As the packet route and timeslot are determined in advance by the arbiter and router, the desired drive current can be transmitted to each SOA module while the previous packet is being sent. Thus the switching speed is ultimately limited by the DAC and SOA, to the order of 20ns.

Our proposed control scheme mitigates the need for high speed optical power meters and ADCs for power equalization by separating the process of sampling the optical power of an incoming packet from the critical period of transmission through the use of calibration and operational phases.

Low latency routing is achieved by confining the equalization process to the calibration period.

Conclusion

A layered approach to control, with modular per-packet power equalisation is shown as a solution to power equalisation in multi-stage SOA switches. A “plug and play” solution for the calibration and control of complex multi device photonic components is a route to enabling their application and commercialisation.

References

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5. T. Lin, OFC2006, paper OWP4