Cambridge startup claims speedier simulation tools

By Peter Clarke
EE Times
(04/24/00, 2:39 p.m. EST)

LONDON — A Cambridge University computer scientist has developed a set of EDA tools that he believes will bring hardware designers world-beating cycle simulation at low cost. The tools also offer a step up to system-level and C-language description for engineers using the Verilog hardware-description language, or reusing legacy designs described in it.

David Greaves, a fellow of Cambridge University's Corpus Christi College, is on one year's sabbatical leave from his position as lecturer in the university's computing laboratory. In that year, which ends in October, he has formed Tenison Technology EDA Ltd. in Cambridge to bring his Verilog-to-C compiler (VTOC) and other tools to market.

Greaves is offering the tools at the relatively low price of $2,000 a year for each customer site and for an unlimited number of seats, at least while the company gets up and running.

"The company's assets are 10,000 lines of ML [a functional language] and a Web site," Greaves said. "I wrote every line of Tenison Technology code over the last five years and much of it has been used for teaching and for other projects in the university and elsewhere."

50x to 100x speed gain

Greaves claimed that his VTOC tool generates a cycle-accurate implementation of a complete Verilog design in the form of a C-language program. The C program can then be compiled and typically runs 50 to 100 times faster than a conventional behavioral simulation, he said.

"Our compiler does not just do a simple translation, though — it goes through all of the steps of a logic synthesizer like Synopsys' but writes out a C program rather than a list of gates," said Greaves. "The C program is a carefully ordered set of assignments to variables, where the variables represent the wires and registers of the Verilog program and the ordering models the behavior of hardware, where inputs are registered before outputs change."

In addition to providing a simulation and debug speedup, Greaves claimed VTOC can be of use to intellectual-property (IP) core licensors. Using VTOC, potential end customers can be provided with object files that protect the IP of the original design, yet enable a full evaluation of the design in a customer application, he said.

"The debugging environments for C and C++ systems are way ahead of those for Verilog," said one beta tester who chose to remain anonymous. "So using VTOC I can debug my hardware design at high speed with the software tools that are used for the rest of our system."

Greaves added: "A final advantage is that, in most sites, Verilog licenses are in short supply, but no license is needed to execute the C generated by VTOC."

Tenison Technology is also planning to offer a C-to-Verilog compiler. The CTOV product will allow complex sections of behavioral code written in ANSI C to be mapped to hardware, with advanced support for multithreading and packing

variables into memories.

Both products use three variants of a set of semantics known as Tenos. A Tenos manual and white papers on the VTOC product are downloadable from the Tenison Web site.

Even though Tenison is currently a "one-man band," Greaves believes the technology will be compelling to ASIC and system developers and eventually find a commercial route to market.

"The most important thing is to develop a core of good-quality algorithms in this area and increase the value of the company's IP," he said. "We are currently selling the licenses for our products at a very low price, just enough to cover support. With any luck the company will be bought by a large player in a couple of years. In the meantime, I hope our customers will find our software really useful."

He added, "If the right person comes along as a potential CEO, then they can join the company and rewrite the business plan."Tenison is using an innovative pricing model for its tools, which can run under the open-source Linux operating system and Sun's Solaris versions of Unix. Greaves promises a Windows NT version "in late summer. CTOV will be the same when it is available."

Typically EDA companies demand tens of thousands of dollars per engineering seat for a leading-edge tool, not the $2,000 Tenison is charging per site per year, regardless of the number of seats.

Greaves said that because the code was not written as part of a sponsored project and did not use significant university resources, Cambridge University has allowed him to retain his IP rights in the work. "In this case I have decided to set up a company and give the IP rights to the company," he said.

Some of the work is being stimulated by Cambridge University's relationships with Microsoft Corp. and AT&T. Both U.S. giants have branches of their corporate R&D operations based within, or close to, the university.

"Tenison's companion CTOV compiler contains a great deal of new research content, especially in the field of symbolic evaluation of multithreaded imperative programs," said Greaves. "There is a large group spread between the department and our associated industrial research laboratories, particularly those of Microsoft and AT&T, exploring the theory and practice of this, mainly for software systems."

"The challenge we are facing, both for hardware synthesis and optimizing compilers, is to make a tool that runs in a reasonable time [and] that can take advantage of the new theoretical techniques. Basically, the new techniques involve searching possible execution paths, and this is an exponential problem," said Greaves.

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