XILINX Teaching Board

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1. Overview

The XILINX Teaching Board is a small (100 x 160mm) PCB which houses a Xilinx logic cell array (LCA) chip, a single chip micro (SCM), four static RAM (SRAM) chips and an RS232 serial interface. The SCM runs a loader program which allows the Xilinx to be programmed by a host computer over the serial interface. All control lines of the SRAM chips are connected the Xilinx I/O pins and there are also 8 LEDs which may be controlled by the Xilinx. The remaining I/O pins of the Xilinx are brought out to an expansion connector.

2. Power Supply

The board requires a DC power supply in the range 7 to 10 volts. A regulator on the board converts this to 5V DC. The power consumption of the board with all LEDs illuminated but with the Xilinx inactive is approximately 150mA. Power is provided via a standard 2.1mm DC supply socket (J1). The outer contact of the socket is the positive rail. The board is protected against reversed supply by a diode (D1) and against excessive current consumption by a fuse (FS1).

3. Single Chip Micro

The single chip micro is a 63701 type. It has an internal EPROM which contains the loader program and 29 I/O pins which control the rest of the board. Two I/O pins form the serial interface and a third drives a LED in the LED display pack. 15 I/O pins are used to control the Xilinx and a further three are used to read configuration information from links on the board. The remaining 8 I/O pins are not used. An oscillator module on the board provides a 4.9152 MHz clock for the SCM and this clock is also fed to the Xilinx.

While the loader program is running the LED driven by the SCM flashes on and off. It is off for approximately 1 second and then flashes twice in quick succession.

4. Serial Interface

The board has an RS232 compatible serial interface which is controlled by the SCM. Connection to the serial port is via a 9 way D plug (J2) with connections as follows.

Pin 2	Rx data (input to board)
Pin 3	Tx data (output from board)
Pin 5	Ground

The loader operates the serial interface at 9600 baud and there is no low-level handshaking. The data format used is 1 start bit, 8 data bits, 1 stop bit. The loader uses ASCII characters for communication and expects bit 7 of each character to be zero.

5. Xilinx Control

The Xilinx is controlled by two 8 bit I/O ports on the SCM. One of these drives 7 Xilinx control lines while it is being programmed and the other supplies the 8 data lines during programming. After programming is complete, these ports may be used to communicate with the Xilinx via the serial interface. Most of the control lines have pull up resistors to ensure that the lines are inactive while the board is powering up. The loader program drives some of the Xilinx control lines and the Xilinx data bus while it is programming or communicating with the Xilinx but the default state of all these lines is undriven.

6. Resetting the Board

The board has a power-on reset circuit to reset the SCM when power is applied. There is also a switch (SW1) which resets the SCM. There is no direct reset to the Xilinx which will perform its own internal reset at power-on. Subsequent resets are provided by the SCM loader which only resets the Xilinx when it receives the appropriate command on the serial interface.

Resetting a powered-up board with the switch will have no effect on the Xilinx unless the loader was performing a command at the time.

7. Xilinx Connections

The board is designed to house a Xilinx LCA in a 132 pin grid array package. Types XC3042 and XC3064 are both suitable, the latter having an extra 14 I/O pins. The 4.9152 MHz clock which drives the SCM is buffered to CMOS levels by a 74HCT04 to provide the signal CLK. This signal drives the Xilinx global clock input pin (TCLKIN) and is also available on the expansion connector.

7.1 SRAM interface

The four SRAM chips are controlled by I/O lines from the Xilinx. They form a memory array with either 8k, 32k or 128k words of memory depending on the type of chips fitted. Each word is 32 bits wide and 32 I/O lines (D0-D31) from the Xilinx are connected to the memory chip data lines. 17 I/O lines (A0-A16) are connected to the memory address lines and 2 I/O lines (CS, WE) are connected to memory control signals. CS is the chip select signal and WE the write enable signal of the memory chips.

Name	Xilinx pin	Name	Xilinx pin	Name	Xilinx pin
D0	P4	D16	B1	A0	B3
D1	N5	D17	C2	A1	B6
D2	P7	D18	C1	A2	A4
D3	P3	D19	A8	A3	B7
D4	N3	D20	B8	A4	A6
D5	L2	D21	C9	A5	C5
D6	K2	D22	B9	A6	B4
D7	K1	D23	A9	A7	B2
D8	K3	D24	B10	A8	A7
D9	L1	D25	A10	A9	G2
D10	M1	D26	C10	A10	H2
D11	D2	D27	B11	A11	A5
D12	D1	D28	B12	A12	B5
D13	E3	D29	C12	A13	C6
D14	E2	D30	C14	A14	F3
D15	E1	D31	D13	A15	G1
				A16	F2
CS	H1	WE	J2		

7.2 LED array

The board contains a pack of 10 LEDs. One LED at the right end of the pack indicates that the board is powered. The LED adjacent to that is controlled by the SCM and normally flashes under the control of the loader program.

The remaining 8 LEDs are controlled by the Xilinx. They are numbered L0 to L7 with L7 at the left hand end of the pack (closest to the expansion connector, J3). A logic one on the appropriate Xilinx pin will cause the LED to be illuminated. Because the Xilinx I/O pins have pull-up resistors, all the LEDs will be illuminated until the Xilinx is programmed and the I/O pins configured as outputs. The correspondence between Xilinx pins and LEDs is as follows.

LED	**Xilinx pin**
L0	P2
L1	J3
L2	G13
L3	F13
L4	E14
L5	F14
L6	F12
L7	E12

7.3 Expansion Connector

The expansion connector (J3) provides access to spare I/O pins on the Xilinx as well as the clock and power rails of the board. If the board is fitted with an XC3042 there are 18 I/O lines (X0-X15, XTL1, XTL2) available on the connector. If an XC3064 is fitted, a further 14 lines (Y0-Y13) are available. Note that in addition to being an I/O pin XTL1 may also be used as the input to the Xilinx alternate clock buffer (BCLKIN).

The pins of the connector are as follows.

J3 Pin	**Name**	**Xilinx Pin**	**J3 Pin**	**Name**	**Xilinx Pin**
1	+5V		2	+5V	
3	CLK	C3	4	(n/c)	
5	X15	J12	6	XTL1	P13
7	X14	H13	8	XTL2	M13
9	X13	H14	10	Y13	A2
11	X12	J13	12	Y12	A3
13	X11	J14	14	Y11	A11
15	X10	K13	16	Y10	A12
17	X9	K14	18	Y9	A13
19	X8	K12	20	Y8	E13
21	X7	L13	22	Y7	F1
23	X6	M14	24	Y6	J1
25	X5	N14	26	Y5	L14
27	X4	P12	28	Y4	P11
29	X3	N12	30	Y3	P9
31	X2	N10	32	Y2	P8
33	X1	P10	34	Y1	N6
35	X0	M10	36	Y0	P5
37	(n/c)		38	(n/c)	
39	0V		40	0V	

8. Loader Protocol

Commands are sent to the loader over the serial interface. Each command takes the form of a single character followed by further optional data characters. When the command has been executed a character is sent in reply followed by optional data characters. Commands may also fail in which case an error character is sent back instead of the normal reply.

Characters which do not represent a valid command are ignored.

Command characters are all alphabetic and may be lower case or upper case. Alphabetic characters in hexadecimal numbers may also be in either case. The commands are:

Command	Send	Data	Reply	Data	Errors
Program	M		M		T
Configure	N	nn	N		T,X
Reset	K		K		
Read	R		R	nn	T
Write	W	nn	W		T,X
Status	S		S	nn	
Revision	L		L	nn	

8.1 Program Command

Command: **M**

Action: Makes Xilinx ready for configuration by asserting RESET- and DONE/PROG lines for approx 20us. Then waits for INIT- line low, RDY/BUSY- line high and LDC- line low with a timeout of 250ms.

Returns: **M** if successful
T if timed out

8.2 Configure Command

Command **Nnn**

Action: Provides a byte of configuration data to the Xilinx. Expects 2 hex characters following the command. These characters denote a byte of data to be written to the Xilinx. If either character is not hex (0-9, A-F, a-f) the command returns an error character and terminates. If the data is good, the loader places the data on the Xilinx data pins and drives the WRT- line low for approx 4us before removing the data. It then waits for the RDY/BUSY- line to go high with a timeout of 2.5ms.

Returns **N** if successful
X if bad hex supplied
T if timed out

8.3 Reset Command

Command **K**

Action: Drives the Xilinx RST- line low for approx 20us

Returns **K**

8.4 Read Command

Command **R**

Action: Drives the Xilinx INIT- line low to signal a read operation. The loader then waits for the RDY/BUSY- line to go high with timeout of 2.5ms. Unless the timeout expires it then reads data from the Xilinx data lines and releases INIT- before returning the data as 2 hex characters.

Note that this command will only be effective if the Xilinx has already been programmed to interact with the SCM as detailed here.

Returns **Rnn** if successful
T if timed out

8.5 Write Command

Command **Wnn**

Action Write a byte of data to the Xilinx. Expects 2 hex characters following the command. These characters denote a byte of data to be written to the Xilinx. If either character is not hex (0-9, A-F, a-f) the command returns an error character and terminates. If the data is good, the loader places the data on the Xilinx data bus and drives the WRT- pin low. It then waits for the RDY/BUSY- line to go high with a timeout of 2.5ms. When RDY/BUSY- goes high or the timeout expires, WRT- is released and the data removed from the data bus.

Note that this command will only be effective if the Xilinx has already been programmed to interact with the SCM as detailed here.

Returns **W** if successful
X if bad hex supplied
T if timed out

8.6 Status Command

Command **S**

Action This command returns the state of the Xilinx control lines. Bits are as follows:

```
     7     6     5     4     3     2     1     0
  +-----+-----+-----+-----+-----+-----+-----+-----+
  |  ?  | HDC | LDC-|INIT-|RDY/ |DONE/| RST-| WRT-|
  |     |     |     |     |BUSY-|PROG |     |     |
  +-----+-----+-----+-----+-----+-----+-----+-----+
```

Note that although some of these signals are driven by the loader from time to time, none of them is driven between commands or during the Status command.

Returns **Snn**

8.7 Revision Command

Command **L**

Action Returns a number relating to the hardware issue and loader version.

Returns **Lnn** (currently L01)