Standard Conditions at the End of Stage 1 (1)
Store Dependent Orders (1)
Machine Power Consumption (1)
Core & Transformer Winding Data (6)
Mains Transformers and Chokes (2)
Setting for type 1000 Tape Readers (1)
Address of 116 and 106 Orders (1)
Valve Equivalents (2)
Relays (1)
Relay Control Circuits (7)
Physical Addresses (65)
Gates and Conditional Numbers (5)
The Significance of Digits in an Order (1)
Control Flip-Flops (1)
The Significance of Letters of the Alphabet (2)
The Functions of EDSAC 2 Chassis (1)
Chassis Power Connections (1)
Chassis Connections

1 - (2)
2 - (1)
3 - (2)
4 - (1)
5 - (8)
6 - (3)
7 - (2)
8 - (2)
9 - (6)
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13 - (11)
14 - (14)
15 - (5)
16 - (2)
17 - (7)
20 - (5)

Input/Output (9)
Decca (3)
Store Layouts (2)
Pulse Lengths
Matrix Outputs (2)
Tester for ECL82 Valves (1)
Simple Core Tester (2)
Output Device Test Unit (5)
Logical Diagram of High-speed Punch (1)

Contents of the Wired Store (8)
Standard Conditions at the End of Stage 1 (1)
Store Dependent Orders (1)
Machine Power Consumption (1)
Core & Transformer Winding Data (6)
Mains Transformers and Chokes (2)
Setting for type 1000 Tape Readers (1)
Address of 116 and 106 Orders (1)
Valve Equivalents (2)
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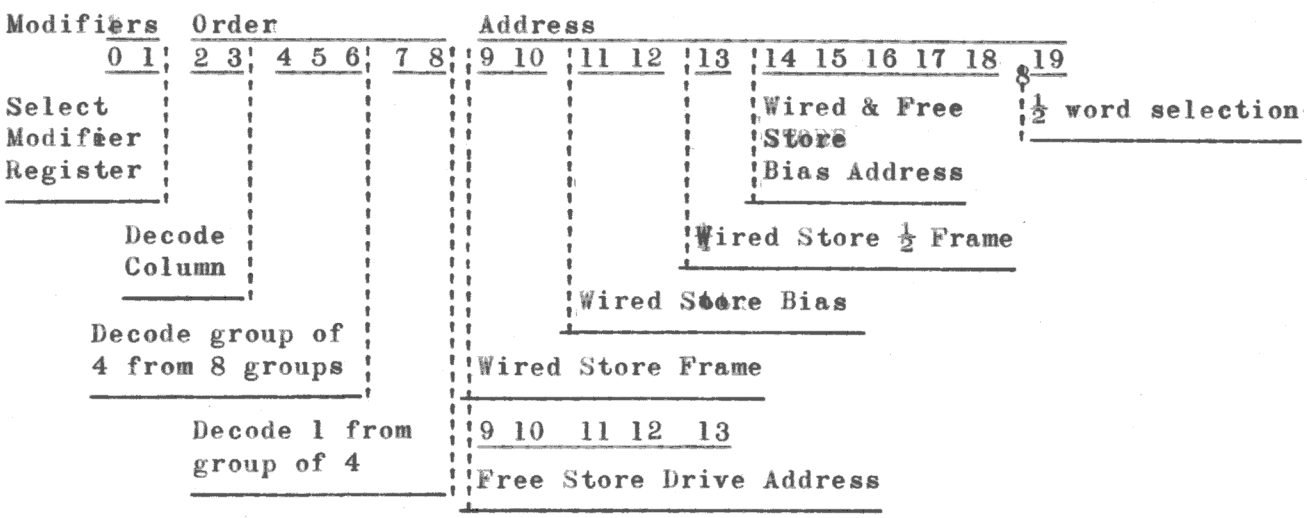
Input/Output (9)
Decca (3)
Store Layouts (2)
Pulse Lengths
Matrix Outputs (2)
Tester for ECL82 Valves (1)
Simple Core Tester (2)

Significance of the Digits in an Order.



Matrix Output and Control Lines.

TTransfer (J) Pulses.

1.	CH		
2.	CcH	Complement of C to H	
3.	KC		
4.	XCN	Characteristic if X to C -	Digits 0 - 31 inclusive
5.	XCE	Exponent of X to C -	Digits 32 - 39 inclusive
6.	FLM	F left shifted to M	
7.	FRM	F right shifted to M	
8.	LMN	Characteristic of L to M -	Digits 0 - 31 inclusive
9.	LME	Exponent of L to M -	Digits 32 - 39 inclusive
10			
10.	MK		
11.	XL		
12.	AC	Activate Constant (Store)	
13.	ELL	E left shifted to L -	Digits 1 - 39 inclusive
14.	ERL	E right shifted to L -	Digits 1 - 39 inclusive
15.	LE		
16.	FN	Characteristic of Sum to F-	Digits 0 - 31 inclusive
17.	EL	E0 and E-1 to L0 and L-1	
18.	MF		
19.	FE	Exponent of Sum to F -	Digits 32 - 39 inclusive
20.			
21.	AX	DigitsFF0 - 8 inclusive to X)	FX
22.	BX	Digits F9 - 19 inclusive to X)	
23.	CX	Digits F20 - 28 inclusive to X)	
24.	DX	Digits F29 - 39 inclusive to X)	
25.			
26.	p	Sum control to p	
27.	0X	Clear X to zeros	
28.	AR	Activat Read (Store)	
29.	AW	Activate Write (Store)	
30.	StX	Output of Store or Constants Matrix to X	
31.	w	Sum Control to w	
32.	tw		
33.	sw		
34.	wt		
35.	Xt		
36.	wq		
37.	rq		
38.	Xq		
39.	ws		
40.	Xs		
41.	wu		
42.	wcu	w complement to u	
43.	Xu		
44.	r	Sum control to r	
45.	pr		
46.	BG	Z3 to G9 and End of Blockmark to G10	
47.	SG	Output Sync to G9 and Input Sync. to G10	
48.	WGT	w to G3, G4, and G5 (Paper tape)	
49.	WGM	w to G6, G7, G8, G11, G12, and G13 (Magnetics)	

The Significance of the Letters of the Alphabet.

	Control.	Arithmetic and Control Registers.	Store.
A	Matrix Address Set Wires.	Long Accumulator	
B			Write Wires in Store.
b		Modifier registers, 'r' 's' or 't' unspecified.	
C	Column Drives.	A.U. Register. holds Multiplicand.	
D		Output Register.	
E		Shift Register of lest significant half of long accumulator.	
F		Shifit Register of Most significant half of long accumulator, also accepts sum of H+M.	
G	General Flip-Flops set and reser by Transfer (J) Pulses.		
H	Conditional Bias Lines.	A.U. Register. complimenting register and one side of adder.	
J	Transfer Pulses, set by 's' and reset by 'K'.		
K	Pulses from main waveform Generator.	A.U. Register for holding multiplicand for accumulative multiplication, also computed sum of data in 118 order.	
L	Line Drives.	Least significant part of long accumulator.	
M		Most significant part of long accumulator.	
N			Pulses from Store waveform Generator, Chassis 5.
p		Store address register.	
q		control register.	
R	Address reset wires.		
r		Sequence control register.	

	Control.	Arithmetic and Control Registers.	Store.
S	Matrix Set Wires for 'J', 'Y', and 'Z'.		
s		Modifier Register.	
T			Store address Row Bias (After primary decoding).
t		Modifier Register.	
X		[illegible]	
U			Store Address Column Drive (after primary decoding).
u		control Register.	
V			Digit Read Out wires for Store.
w		Control Register.	
X			Store Register.
Y	Flip-Flops set and reset by 's' and controlling route through the Matrix.		
Z	Flip-Flops set and reset by 's' and controling Arithmetic and Control Functions.		

The Functions of Edsac 2 Chassis.

Chassis No.	No. in Machine	Function.
1	40	Circuits for handling Arithmetic operations for a single digit whose significance is 2^{-nn} where n is the digit no.
2	11	Circuits for handling Control operations for a single address digit whose significance is 2^{n} where n is the digit no.
3	20	Circuits for handling store, read and re-write; input, and output. The chassis handles 2 digits of significance 2^{-n} and $2^{-(n+20)}$.
4	1	Store Primary decoder.
5	1	Store Waveform Generator.
6	12	Control Matrix Address Flip-Flops, also some 'Z' Flip-Flops.
7	12	Transfer Pulse Flip-Flops.
8	3	Conditional Bias Amplifiers.
9	1	Control Waveform Generator.
10	2	Miscellaneouse 'G' Flip-Flops.
11	2	Input and Output Control.
12	~~8~~	~~Cathode Follower Units for Transfer Pulses.~~
13	1	Magnetic Tape Store Colck.
14	2	Magnetic Tape Store, Tape Control Circuits.
15	1	Magnetic Tape Store, Read Statisisors.
16	2	'Y', and some 'Z' Flip-Flops.
17	1	Start / Stop and Function Decoder Row Drive.
18		
19		
20		
21	8	Magnetic Tape Store Amplifiers.
21a	8	Magnetic Tape Store Amplifeer Sub-chassis.

CHASSIS POWER CONNECTIONS.

1. E	2. H	3. H	4. H	5. -6M	6. -165M
7. +300	8. H	9. H	10.H	11.-300A	12.-300B
13.+150	14.+100	15.+50	16.-150	17.-300	18.X
19.+250	20.X	21.X	22.X	23.X	24.X

Variable Connections.

Pin No.	Chassis No. 1	2	3	4	5	6	7	8
18			+20M		+20M			
20	E'	E'	E'	-1L				
21				1L	-450			
22			-150A	-1R	-150A	-150A		
23			-150B	+1R	-150B	-150B		
24	-12	-12	-12	-12	-12		Cathdde Follower Bias	

Pin No.	Chassis No. 9	10	11	12	13	14	15	16
18						Discriminator Level		
20		E'	E'			E'		
21	-450	Neon		-450				
22		Neon	-150A					-150A
23			-150B					-150B
24		-12	-12	-12				