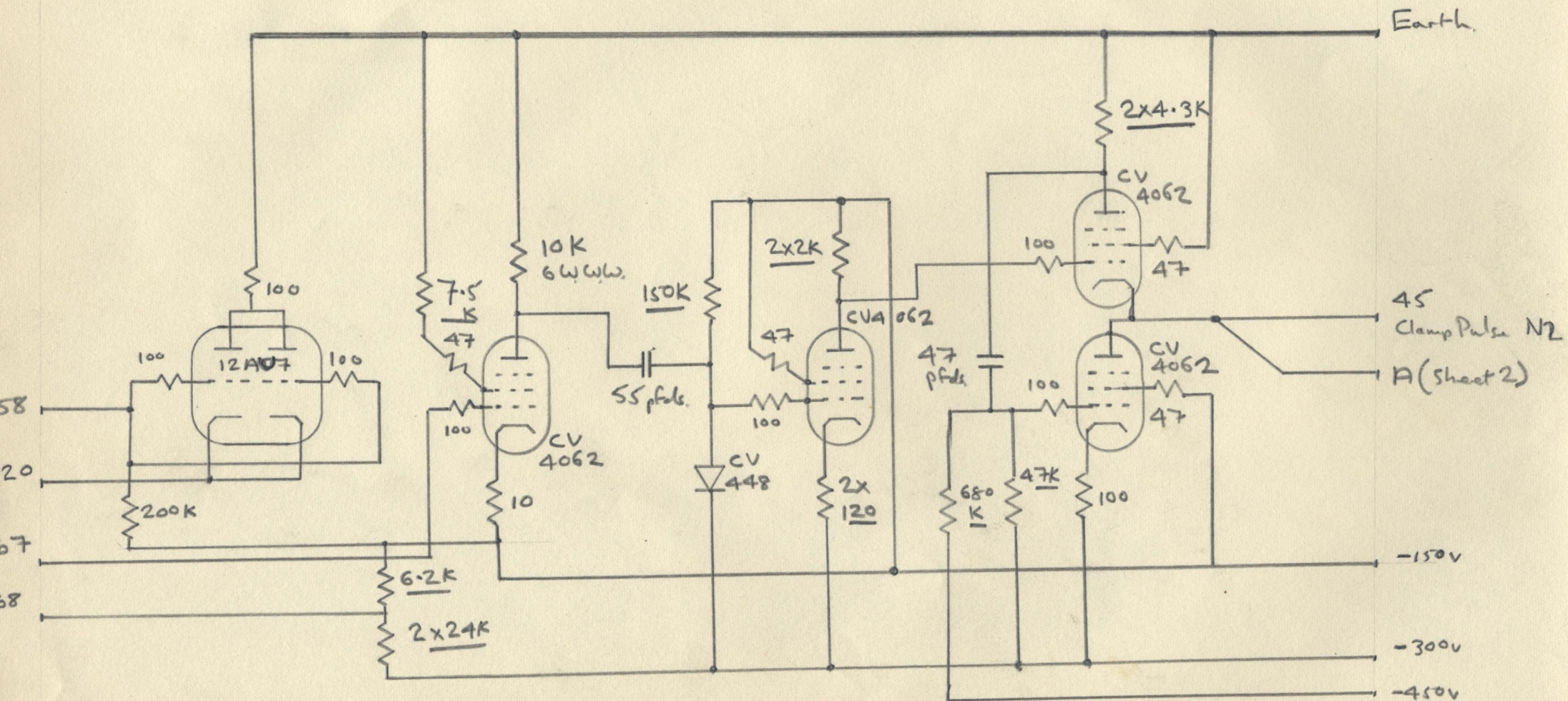


CHASSIS V.

<u>Inputs.</u>		<u>Outputs.</u>	
<u>Pin No.</u>	<u>Source.</u>	<u>Pin no.</u>	<u>Designation.</u>
25	J29 AW	29	B40 Write currnt to Store.
26	J28 AR	30	Parity from store Neon.
27	-V40	31	N4 Bias control wffm.
33	+V40	32	N5 Drive pulse
35	J27 OX	36	Parity input Neon.
41	N6 OX	42	N6 OX
43	N1 Write pulse.	44	N1 Write gate pulse.
46	N2 Amp. gate.1	45	N2 Amp. gate pulse 1.
47.	N3 Amp. gate 2.	48	N3 Amp. gate pulse 2.
58	J30 StX	64	OX X-
61	Parity Input	65	X+
	See note.	66	See note 2.
		72	Parity check out.
N1	Writing current gate pulse.		
N2	Amplifier Gate pulse 1.		
N3	Amplifier Gate pulse 2.		
N4	Bias control Waveform.		
N5.	Drive Pulse.		
N6	Reset pulse for Store register X		
J27	Activate Clear X. N6		
J28	Activate Read N4 and N5.		
J29	Activate Write N4 and N1.		
J30	Store to Store register N2 and N3.		

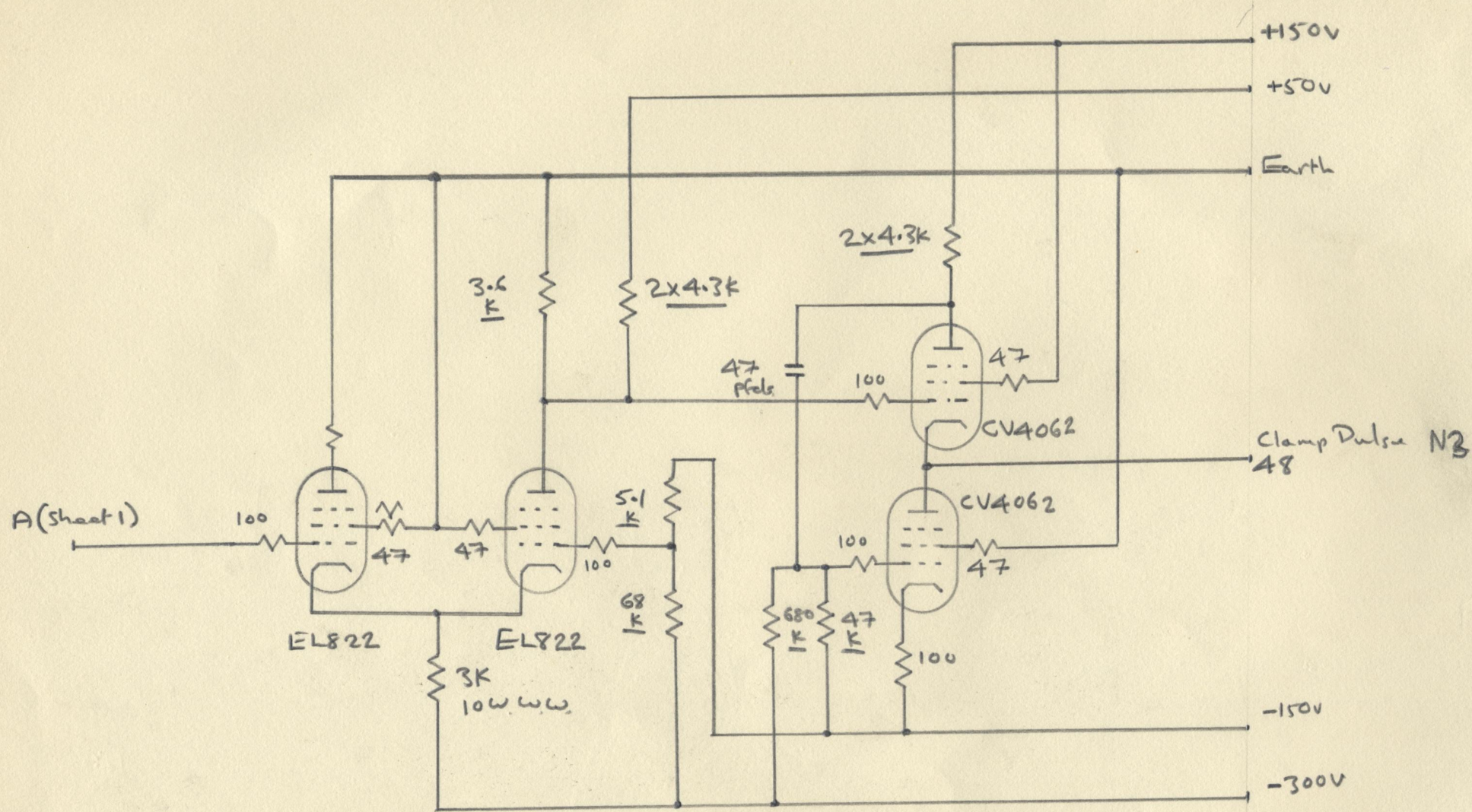
Notes.

1. Pin 61 (Parity In) connected to Parity Out, Pin 66 of Chassis III, digit 5, designated Parity out.
2. Pin 66 - Write pulse high protection cct. connected to H.T. Interlock.



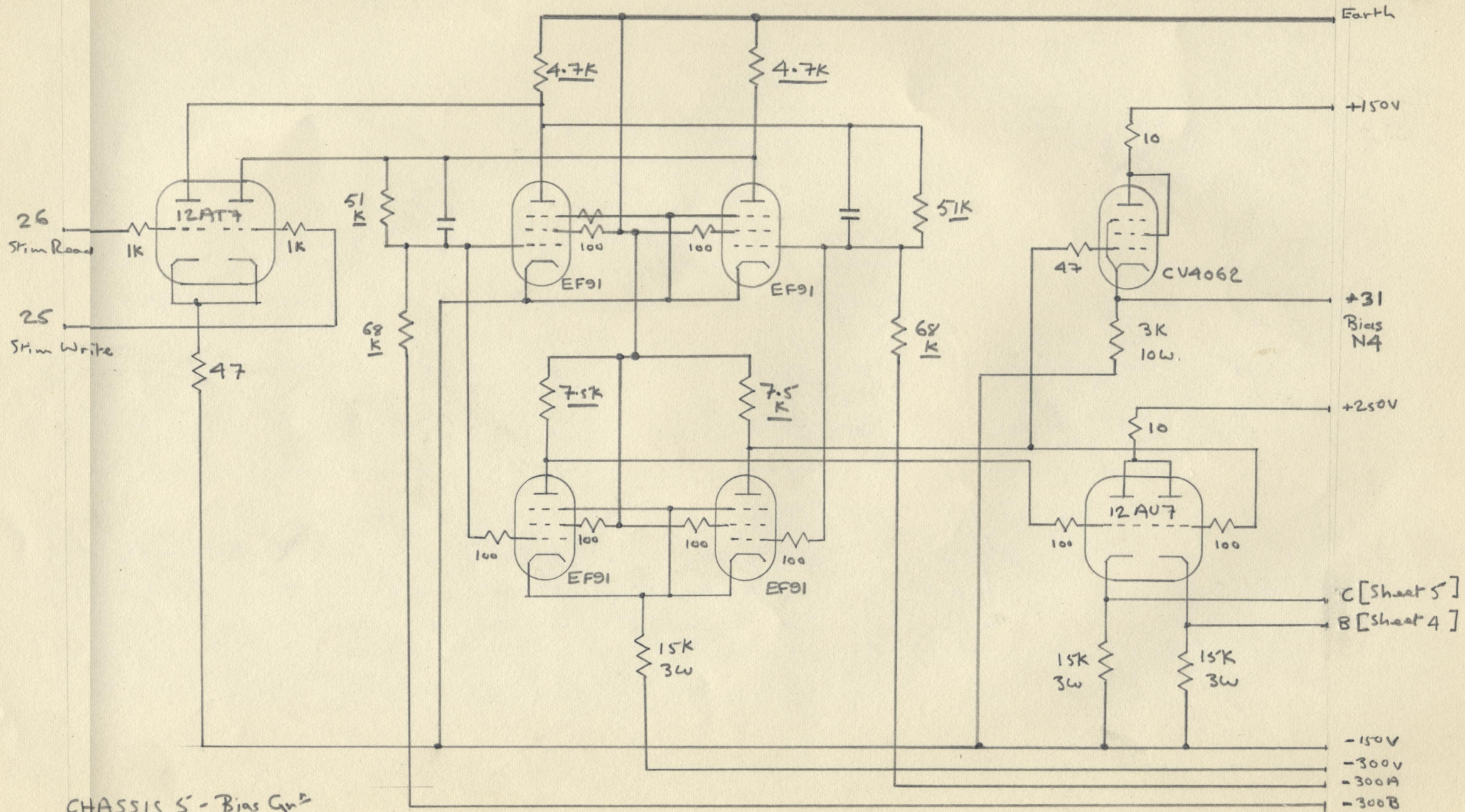
CHASSIS 5 - Clamp Pulse Genr 1.

Sheet 1 of 5 Sheets.

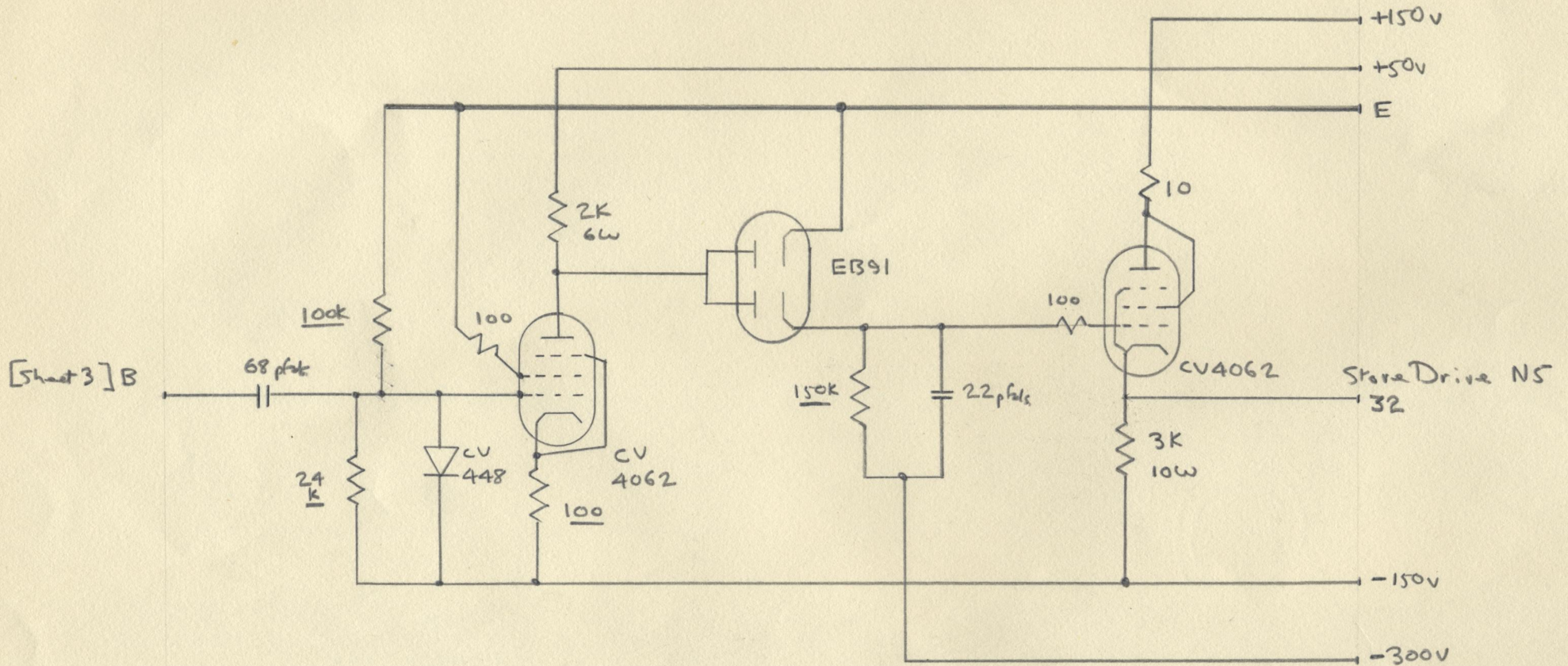


CHASSIS 5 - Clamp Pulse Gen' 2.

Sheet 2 of 5 Sheets.

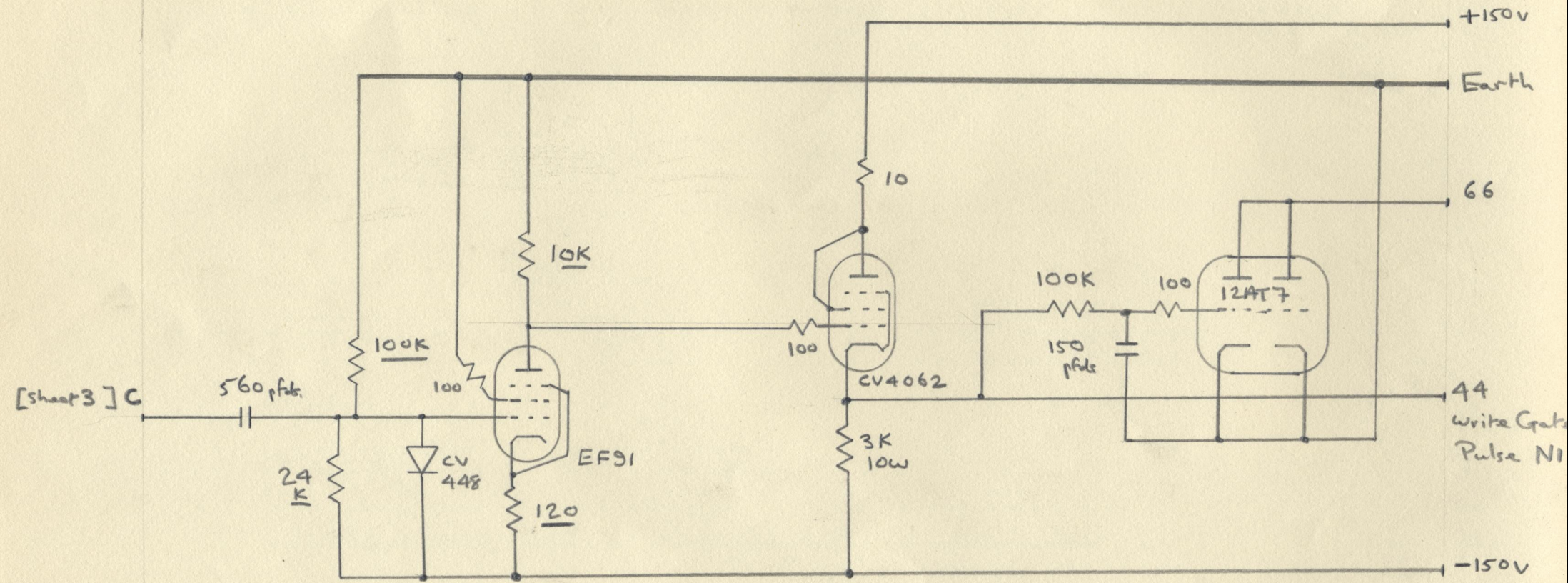


CHASSIS 5 - Bias Gr^d
 [Sheet 3 of 6 sheets]



CHASSIS 5 - Store Drive Pulse Gen

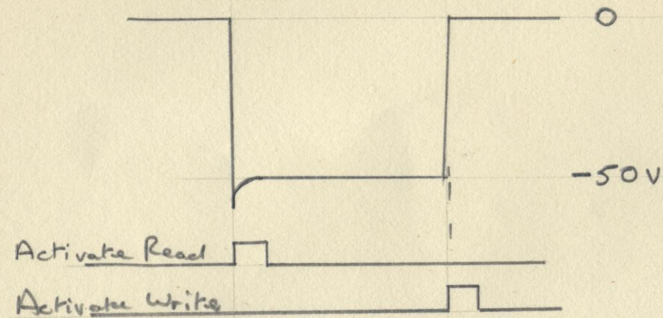
Sheet 4 of 6 Sheets.



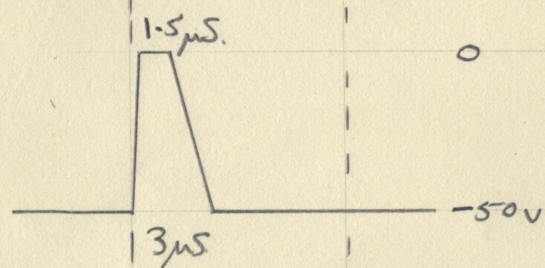
CHASSIS 5 - Write Gate Pulse Gen

Sheet 5 of 6 Sheets.

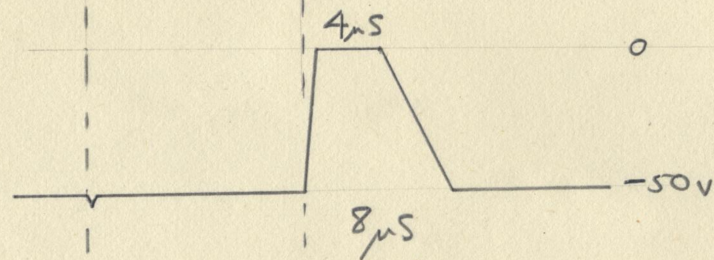
Store
Bias
N4



Store
Drive Pulse
N5

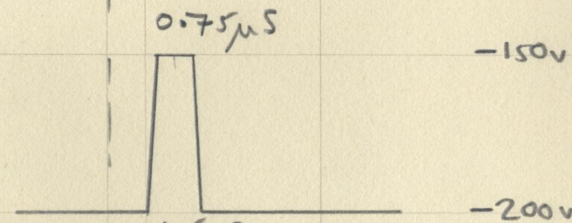


Store
Write Gate
Pulse
N1

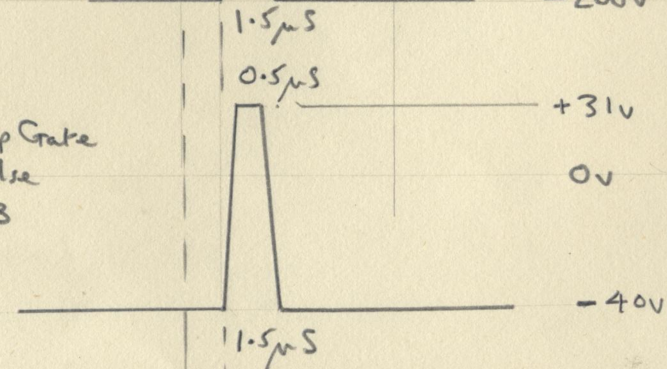


ST $\rightarrow$ X

Amp Gate
Pulse
N2



Amp Gate
Pulse
N3



approx
1 μ Sec. Delay

CHASSIS 5 - Waveforms.

Sheet 6 of 6 Sheets.

