v0

# CHASSIS III.

Sheet 1.

## Inputs

| Pin No. | Source |
|---|---|
| 27 | −V0---19 |
| 28 | −V20--39 |
| 33 | +V0---19 |
| 34 | +V20--39 |
| 37 | J56 |
| 38 | J21, J22, (See note 1) |
| 39 | J23, J24, (See note 1) |
| 40 | J57 |
| 41 | N6 |
| 42 | −Z6 |
| 43 | N1 |
| 44 | −I20--39 |
| 45 | +I20--39 |
| 46 | N2 |
| 47 | N3 |
| 48 | +Z6 |
| 49 | −Z5 |
| 50 | −I0---19 |
| 51 | +I0---19 |
| 54 | +G2 |
| 55 | +Z5 |
| 56 | −W (See note 2) |
| 57 | +W (See note 2) |
| 60 | −G2 |
| 61 | Parity in 1. (See note 3). |
| 62 | −F20--39 |
| 63 | +F20--39 |
| 67 | Parity in 2, (See note 3) |
| 68 | −F0---19 |
| 69 | +F0---19 |

## Outputs

| Pin No. | Designation |
|---|---|
| 29 | B0---19 |
| 30 | B20--39 |
| 52 | −D20--39 |
| 53 | +D20--39 |
| 58 | −D0---19 |
| 59 | +D0---19 |
| 64 | −X20--39 |
| 65 | +X20--39 |
| 66 | Parity 2 out. (See note 3). |
| 70 | −X0---19 |
| 71 | +X0---19 |
| 72 | Parity 1 out, (See note 3). |

## Neon Outputs.

| | |
|---|---|
| 25 | D0---19 |
| 26 | D20---39 |
| 31 | X0----19 |
| 32 | X20---39 |

N2, N3, N6 are clock phases.
G2 Output gate lane steering
[Z2 Address adder Cin]
Z5 Input select (mill vs address unit)
Z6 Enable non-zero data to RX
JJ21-24 AX--DX in some perm
JJ56 IX, JJ57 XD (AO)

## NOTES

1. a) J21 is connected to pin 38 digits 0/20 to 8/28
   J22 is connected to pin 38 digits 9/29 to 19/39

   b) J23 is connected to pin 39 digits 0/20 to 8/28
   J24 is connected to pin 39 digits 9/29 to 19/39

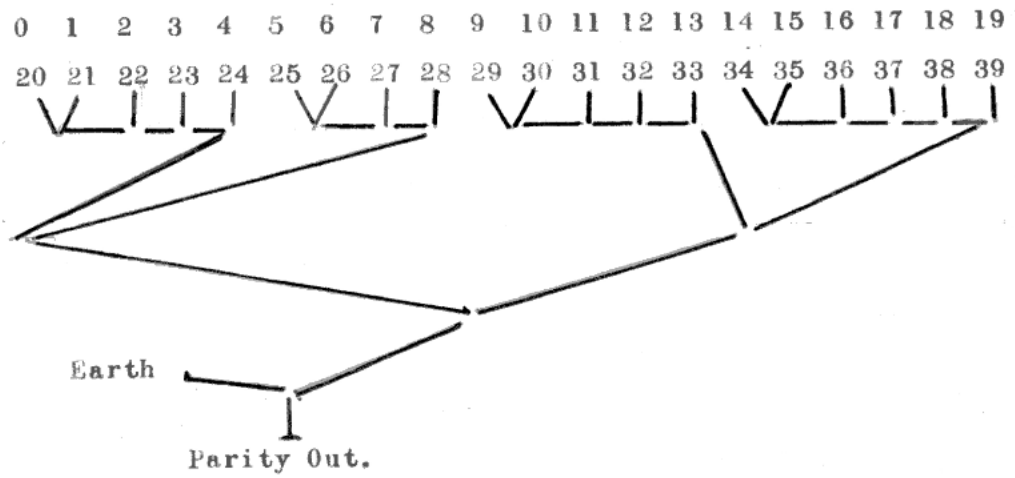
2. $+w_{11}$ to $+w_{19}$ are connected to pin 57, digits 0 to 8 and 11 to 19
   $-w_{11}$ to $-w_{19}$ are connected to pin 56, digits 0 to 8 and 11 to 19
   $+w_9$ and $+w_{10}$ are connected to pin 57, digits 9 and 10
   $-w_9$ and $-w_{10}$ are connected to pin 56, digits 9 and 10

3. For Parity Circuit connectins see Sheet 2.

CHASSIS III.



| Chassis No. | Designation. | | Source. | |
|---|---|---|---|---|
| | Pin 72 | Pin 66 | Pin 67. | Pin 61 |
| 0 | 0 | 0-8 | 0-4 | 5-8 |
| 1 | 1 | 0-1 | 1 | 0 |
| 2 | 2 | 0-2 | 2 | 0-1 |
| 3 | 3 | 0-3 | 3 | 0-2 |
| 4 | 4 | 0-4 | 4 | 0-3 |
| 5 | 5 | Parity out | Earth | 0-19 |
| 6 | 6 | 5-6 | 6 | 5 |
| 7 | 7 | 5-7 | 7 | 5-6 |
| 8 | 8 | 5-8 | 8 | 5-7 |
| 9 | 9 | 0-19 | 0-8 | 9-19 |
| 10 | 10 | 9-10 | 10 | 9 |
| 11 | 11 | 9-11 | 11 | 9-10 |
| 12 | 12 | 9-12 | 12 | 9-11 |
| 13 | 13 | 9-13 | 13 | 9-12 |
| 14 | 14 | 9-19 | 14-19 | 9-13 |
| 15 | 15 | 14-15 | 15 | 14 |
| 16 | 16 | 14-16 | 16 | 14-15 |
| 17 | 17 | 14-17 | 17 | 14-16 |
| 18 | 18 | 14-18 | 18 | 14-17 |
| 19 | 19 | 14-19 | 19 | 14-18 |

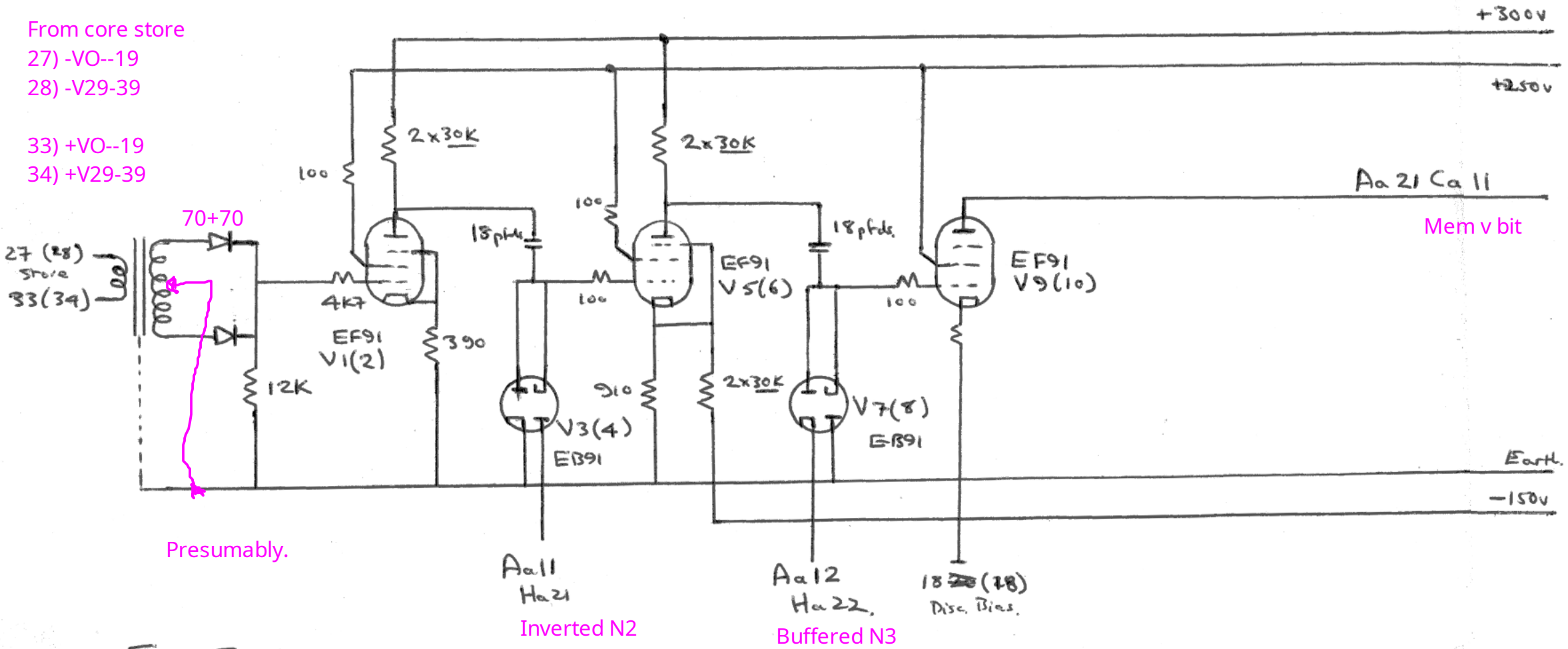


M(L)

CT3/3 (A)

From core store
27) -VO--19
28) -V29-39

33) +VO--19
34) +V29-39




Presumably.

Inverted N2

Buffered N3

Input Transformers.

Spiral Cores. Permalloy 'D' 1" O.D. (STC. WP 2696)
Insulated ½" wide P.V.C. Tape.

Secondary 365 S.W.G. Enam. Cu. Wire. 70+70 Turns

Primary 7/40 Screened P.V.C. Flex } 7 Turns.
P.V.C. Sheathed

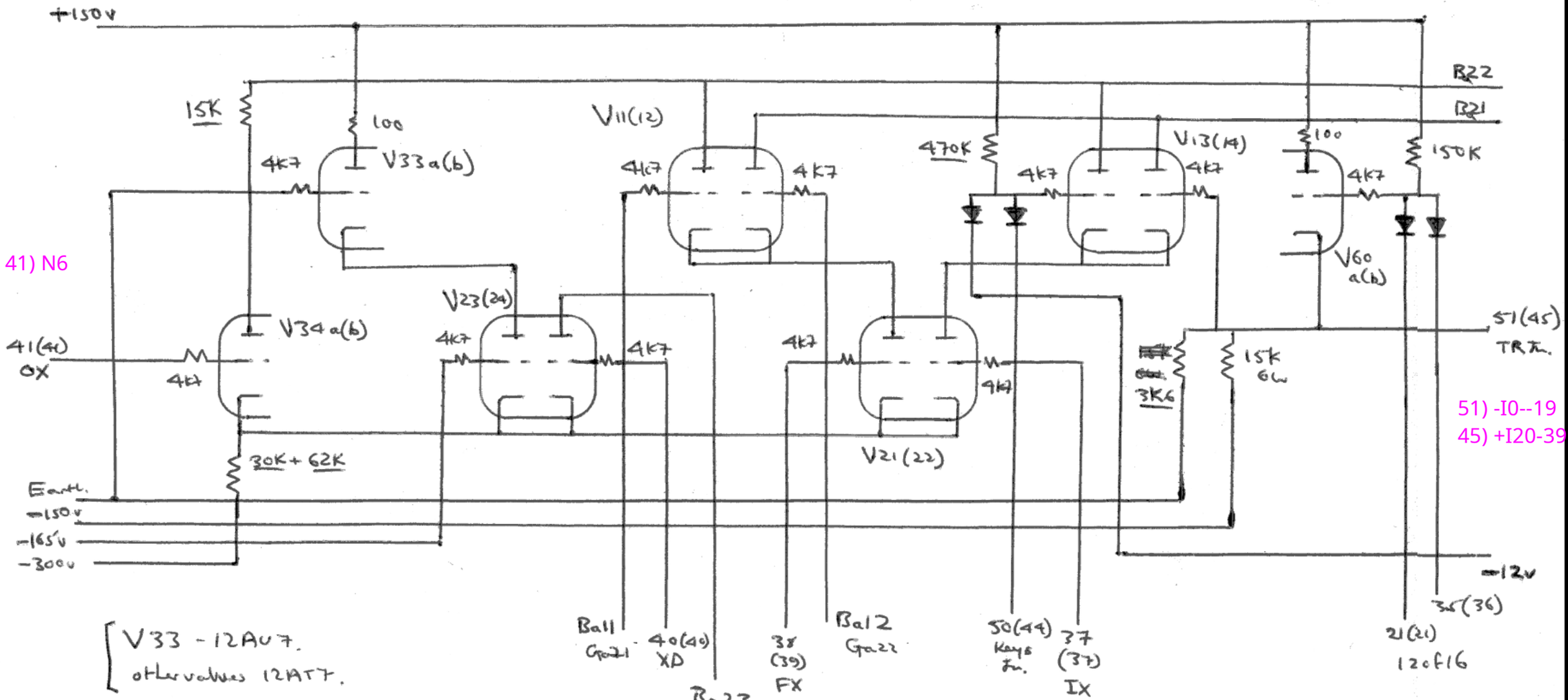
Both windings equally distributed.

CHASSIS 3 - Store Amplifier.

Aa

m(1)

CT3/4 (B)



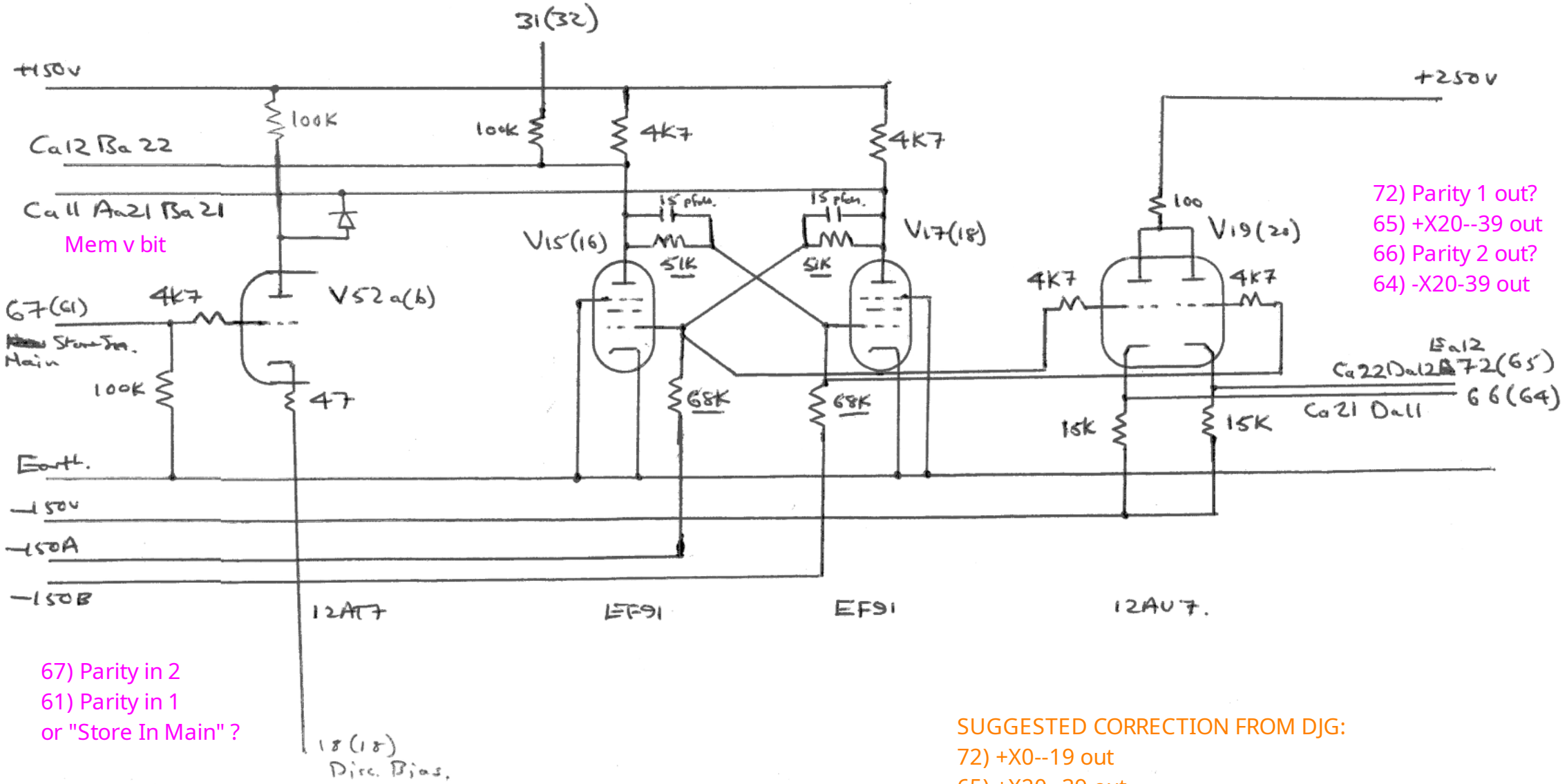

[V33 - 12AU7.
othervalves 12AT7.

CHASSIS 3 - Inputs to X.

Ba

m(l)

CT3/5 (C)




72) Parity 1 out?
65) +X20--39 out
66) Parity 2 out?
64) -X20-39 out

67) Parity in 2
61) Parity in 1
or "Store In Main" ?

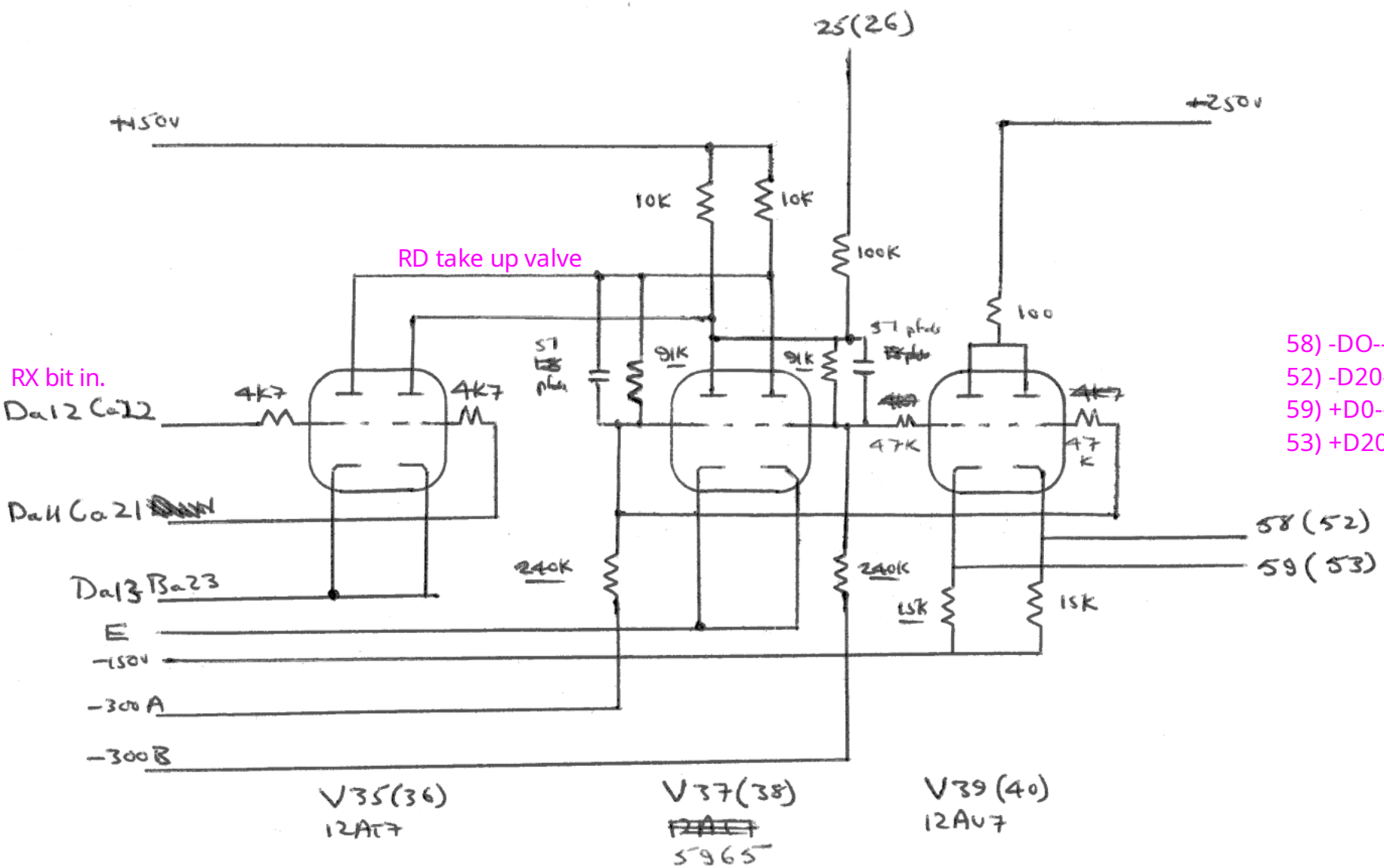
SUGGESTED CORRECTION FROM DJG:
72) +X0--19 out
65) +X20--39 out
66) -X20--39 out
64) -X20-39 out

CHASSIS 3 - 'X' Flip-flop.

C9

m(l)

CT3/6 (D)



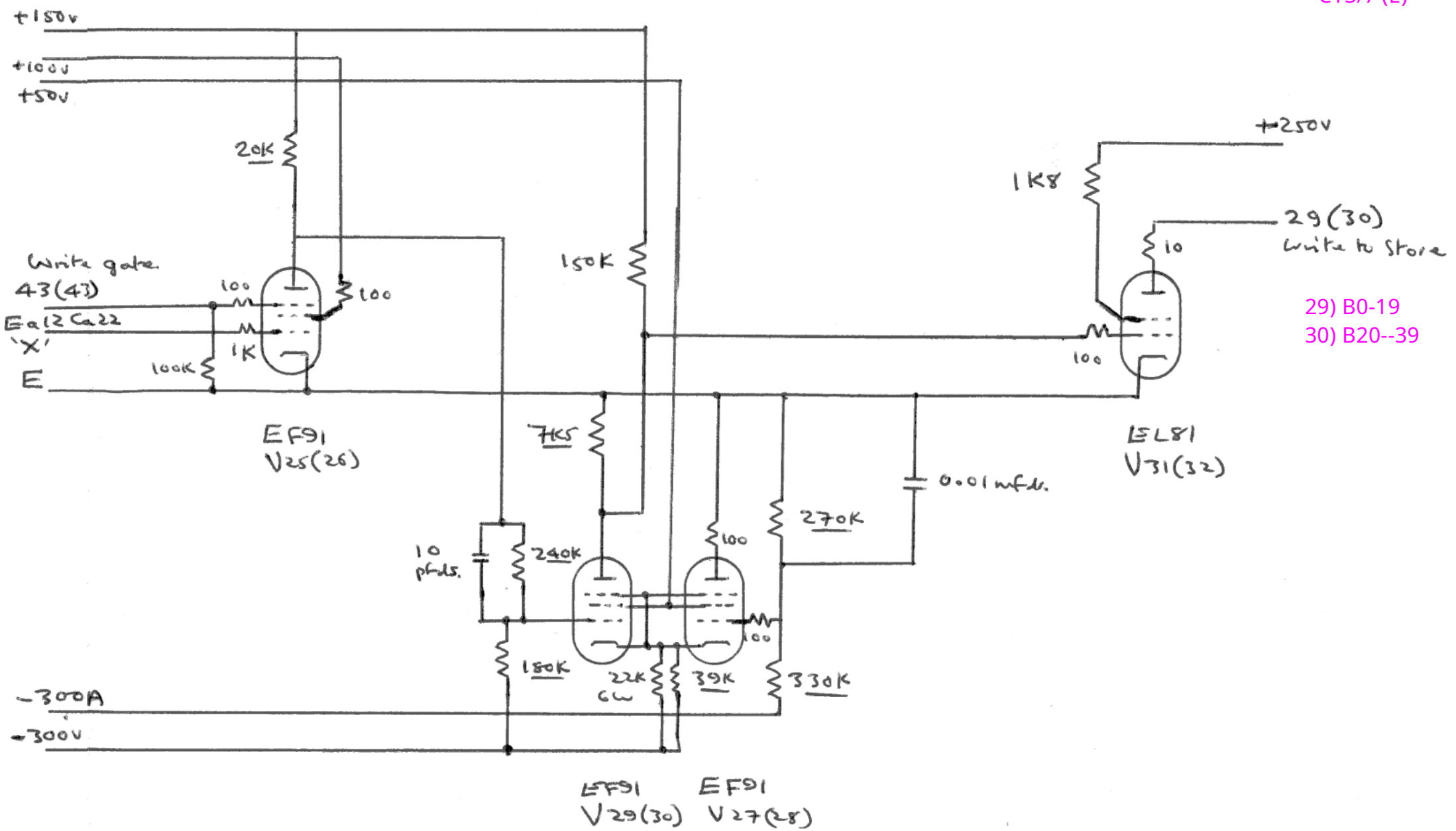

58) -DO--19
52) -D20--39
59) +D0--19
53) +D20--39

The 40-bit RD register is for peripheral output data from the CPU, written by AO micro-command.

CHASSIS 3 - D flip-flop.

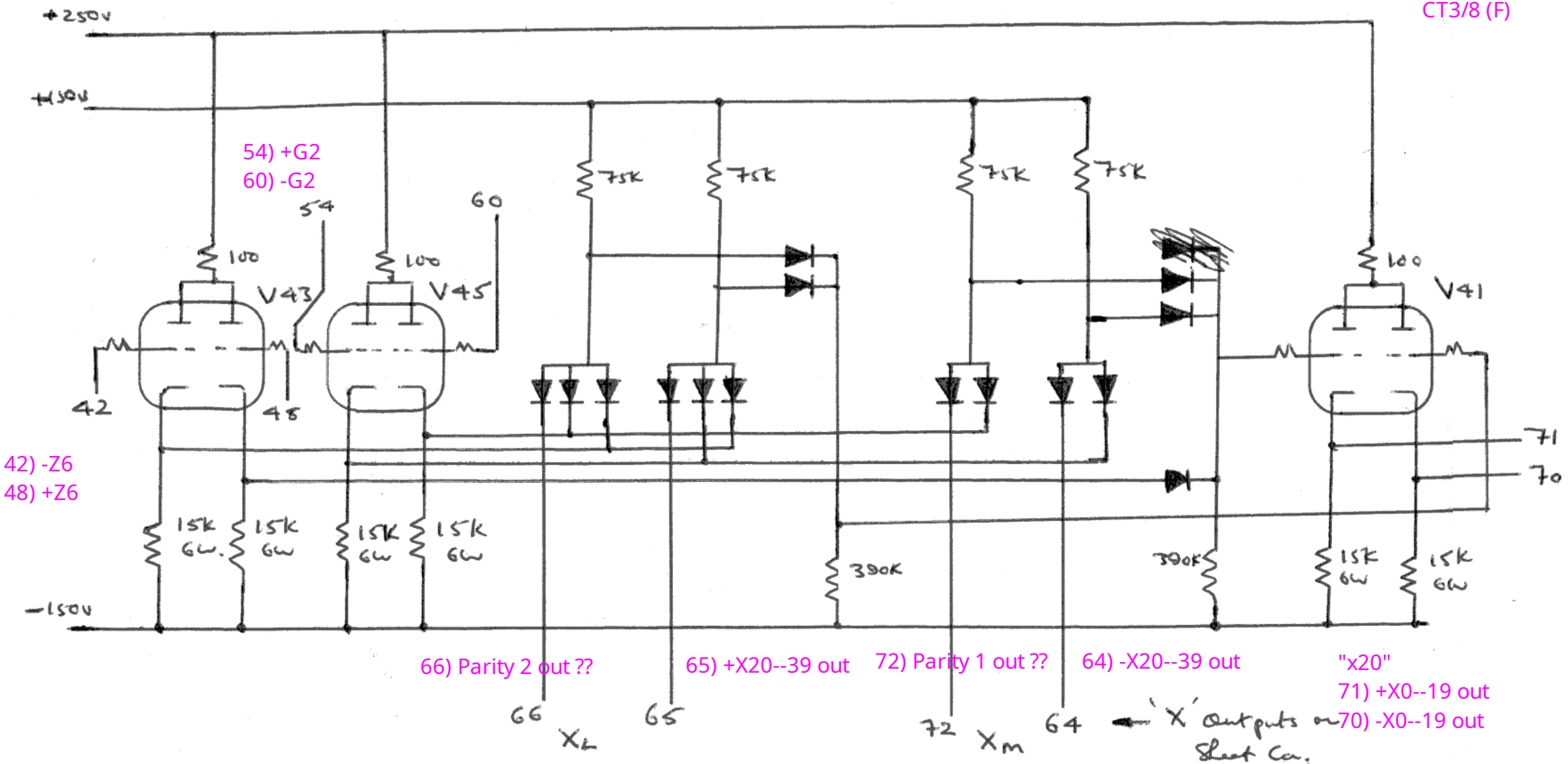
m(l)

CT3/7 (E)




CHASSIS 3- Write Cats.

Ea




This Cct. once only per chassis
All valves type 12AU7.

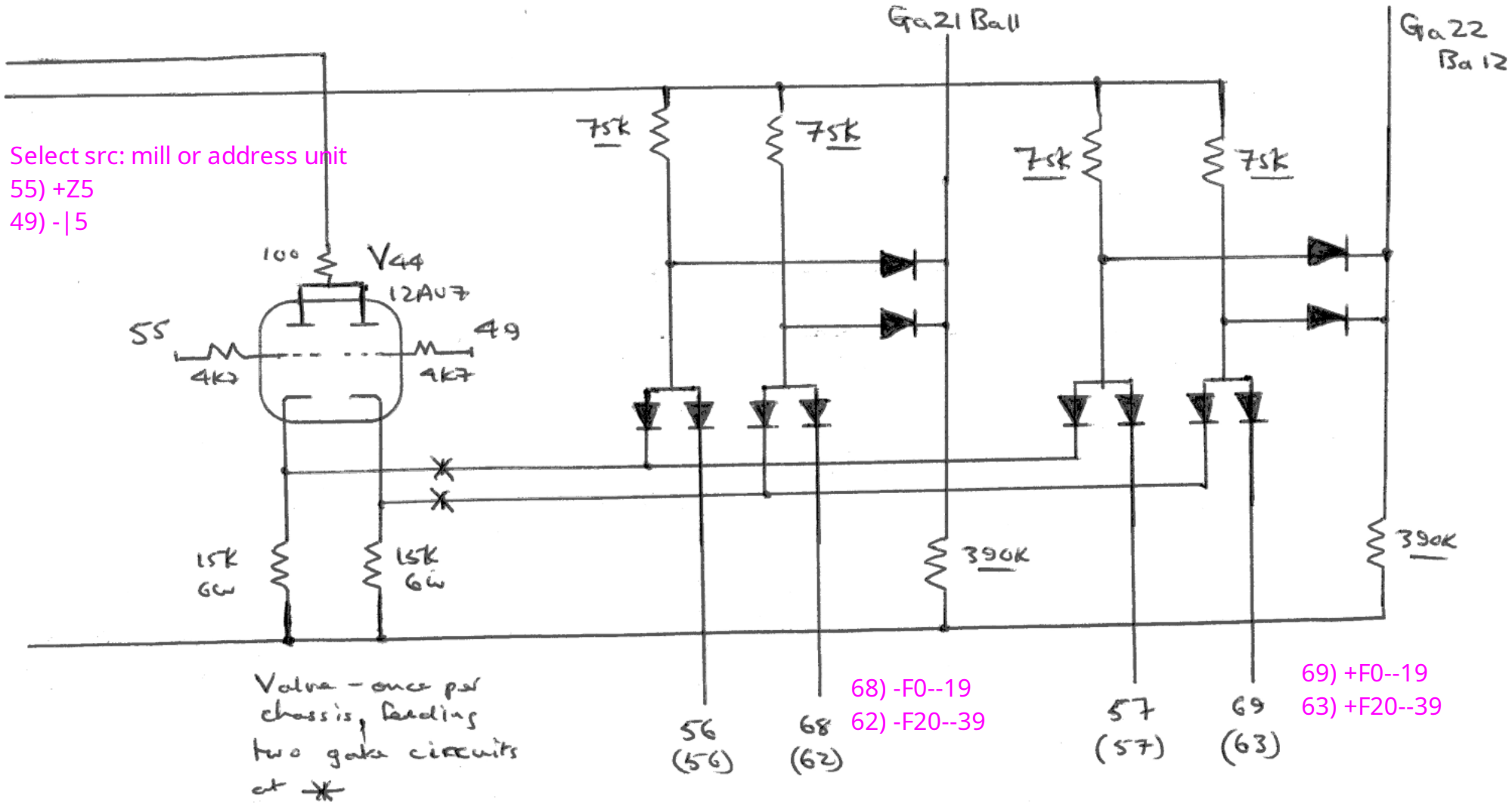
Grid Stoppers 4K7.

CHASSIS 3 - Output Gates.

Pin names in DJG pink from cover page.

SUGGESTED CORRECTION FROM DJG:
72) +X0--19 out
65) +X20--39 out
66) -X20--39 out
64) -X20-39 out

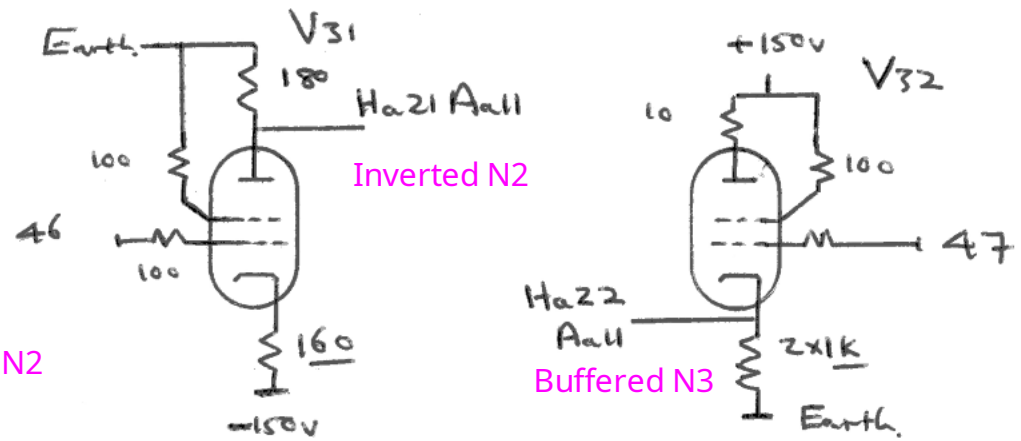
Fa




Select src: mill or address unit
55) +Z5
49) -|5

57) +W + W[e11..19] are connected to pin 57, digits 0 to 8 and 11 to 19
56) +W - W[e11..19] are connected to pin 56, digits 0 to 8 and 11 to 19
57) +W +W[e9..10] are connected to pin 57, digits 9 and 10
58) -W - W[e9..10] are connected to pin 56, digits 9 and 10.

CHASSIS 3 - Input Gate.




46) Clock N2

47) Clock N3

Buffered N3

Circuits once only per Chassis.

Valves type A2134

CHASSIS 3 - Strobe drives.