CHASSIS II.

Inputs

Pin No.	Source
39	ω_q (J37)
40	ω_q (J36)
41	ω_{cu} (J42)
42	ω_u (J41)
43	ω_r (J45)
44	ω_w (J32)
45	ω_w (J33)
46	$+r$ (J44)
47	$+p$ (J26)
48	$+\omega$ (J31)
49	ω_t (J34)
50	ω_s (J39)
51	X_u (J43)
52	X_q (J38)
53	X_t (J35)
54	X_s (J40)
70	$-X$
71	$+X$
72	Carry in, $+Z_2$ (See note)

Outputs

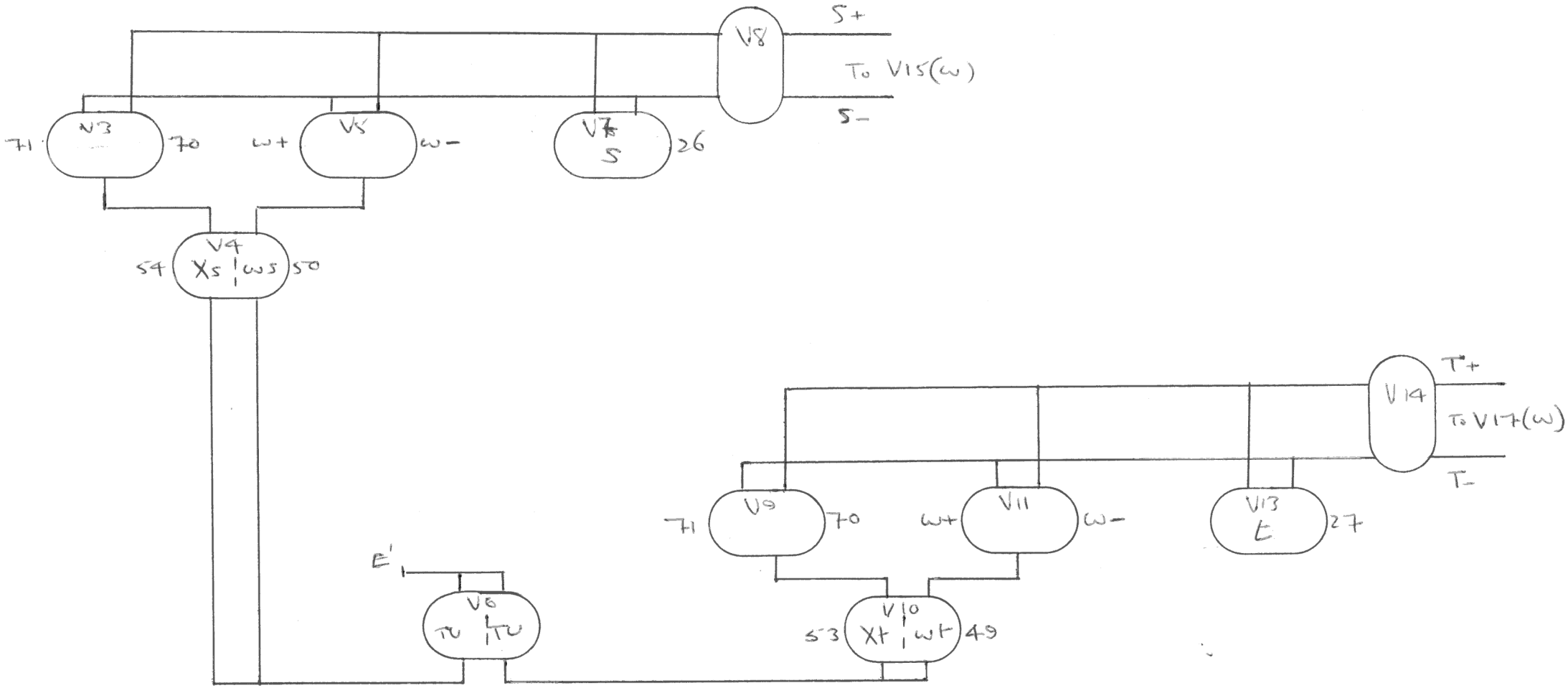
Pin No.	Designation
60	+ p
66	- p
67	Carry out
68	- w
69	+ w

Neon Outputs.

25	q
26	s
27	t
28	u
29	p
30	w
31	r
32	+
33	Cy

NOTE

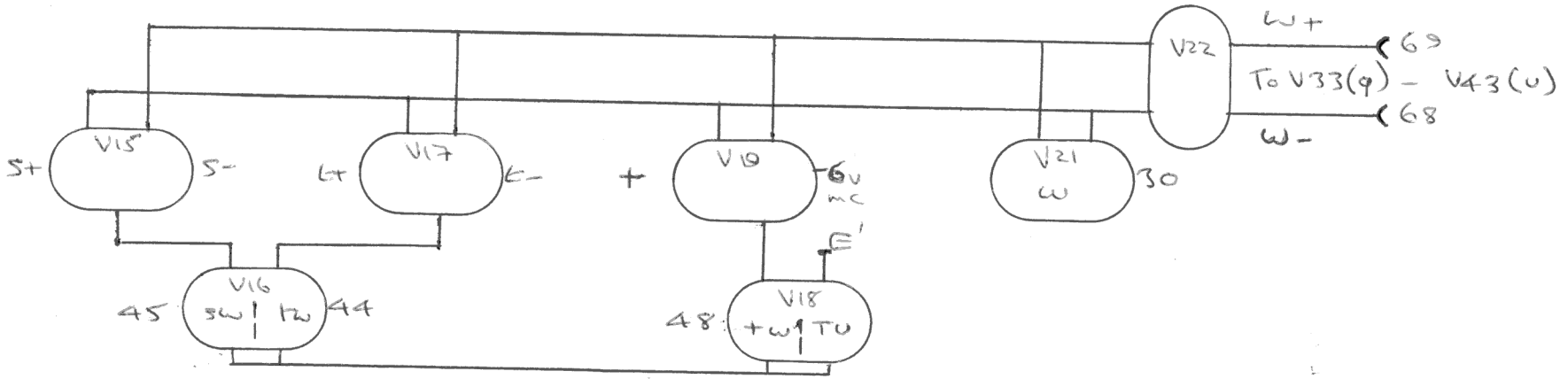
a) $+Z_2$ is connected to pin 72 of Digit 19.
b) Pin 72 is connected to pin 67 of next less significant digt for digits 18 to 9.

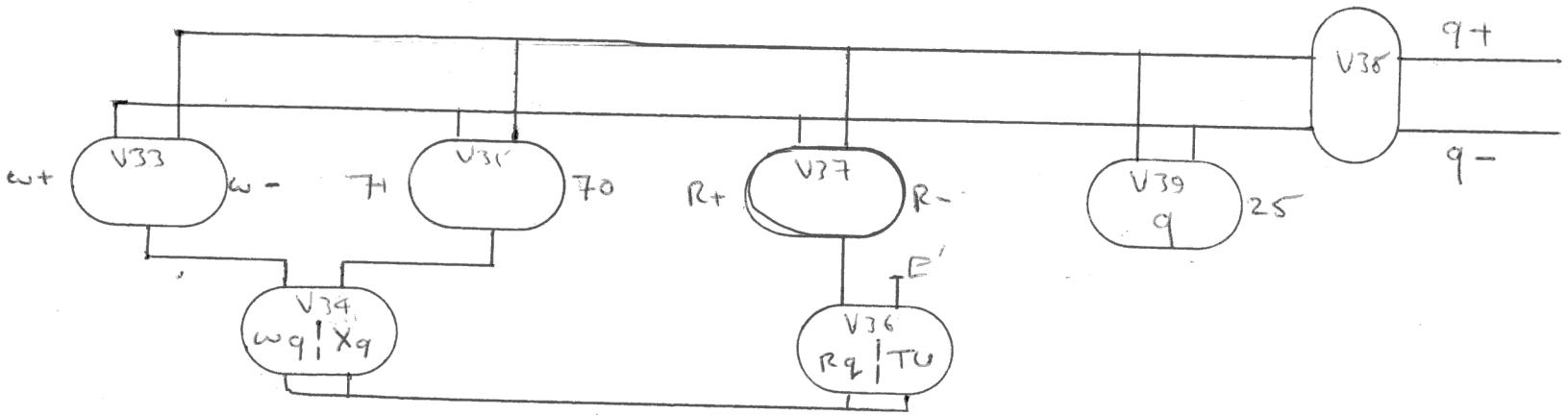

V8
S+
To V15(ω)
S−
V3
71
70
ω+
V5
ω−
V7
S
26
V4
54
X5
ω5
50
V14
T+
To V17(ω)
T−
V9
71
70
ω+
V11
ω−
V13
E
27
E'
V6
TU
TU
V10
53
Xt
ωt
49

Chassis 2

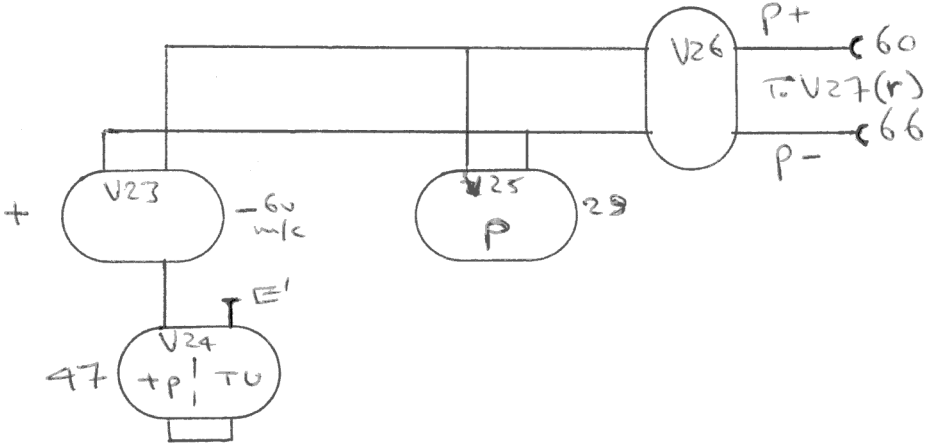
ES

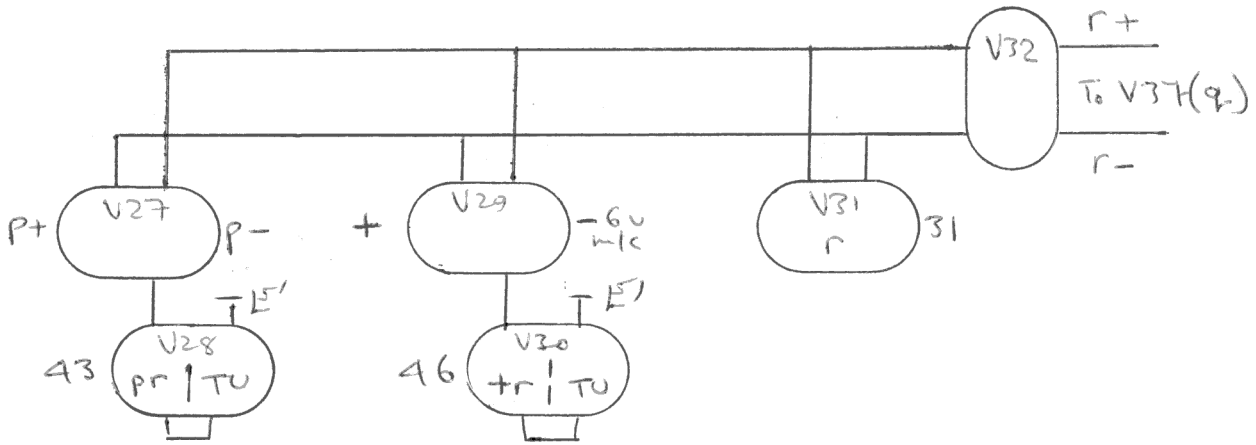
—


V22
ω+
69
To V33(9) – V43(U)
68
ω–
V15
S+
S–
V17
L+
L–
+
V19
6V
mc
V21
ω
30
E'
V16
45
sω | rω
44
V18
48
+ω | TU


V38
9+
9–
ω+
V33
ω –
71
V31
70
R+
V37
R–
V39
9
25
E'
V34
ωq | Xq
V36
Rq | TU

Chassis 2
ω
9





Chassis 2

P

r

3

Chassis 2

$\frac{u}{+}$

4