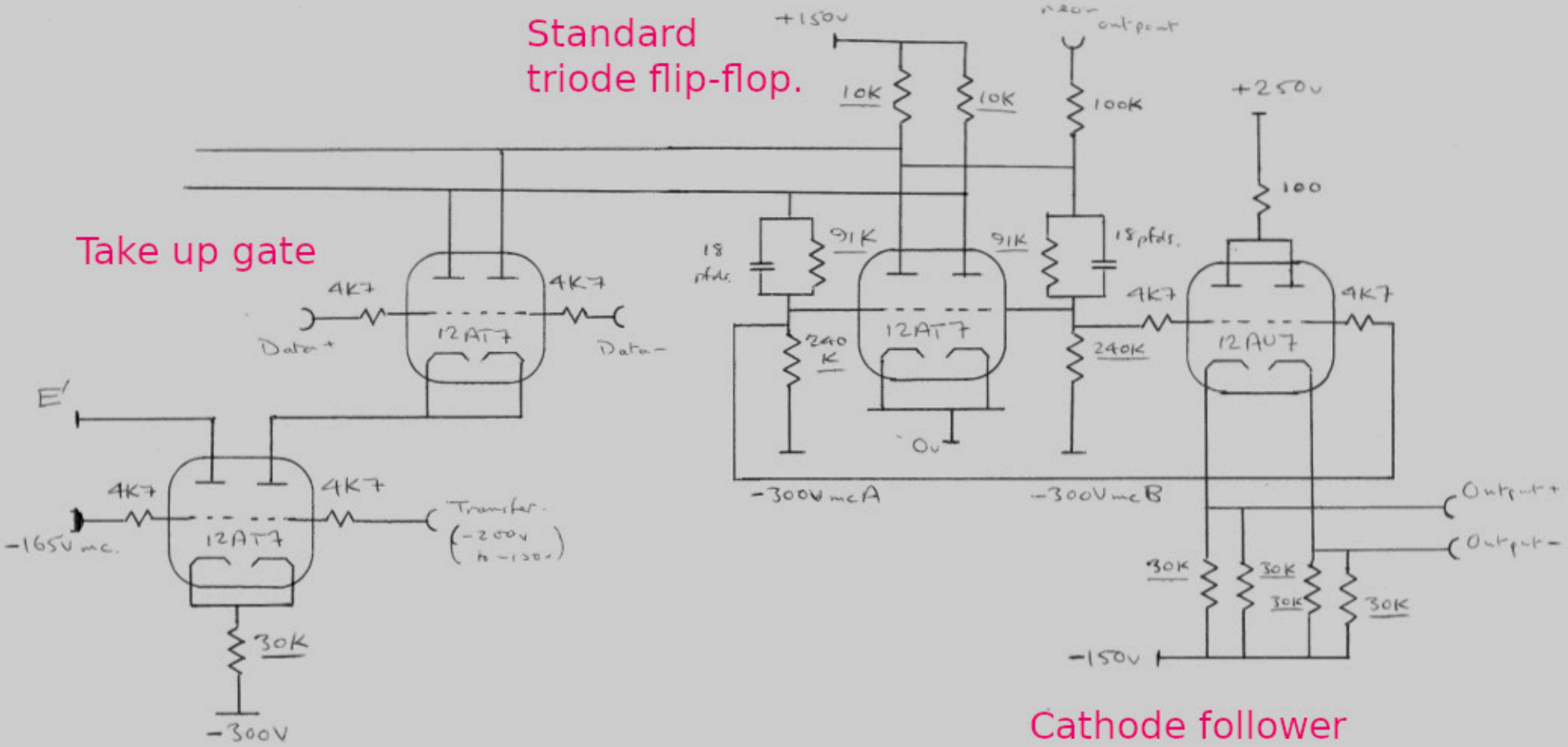
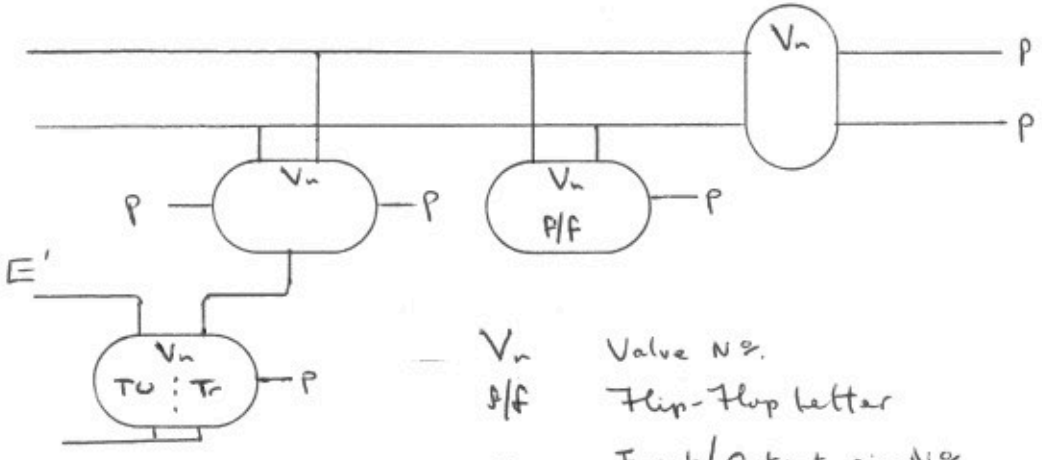


For diagramitic form of this circuit see 2

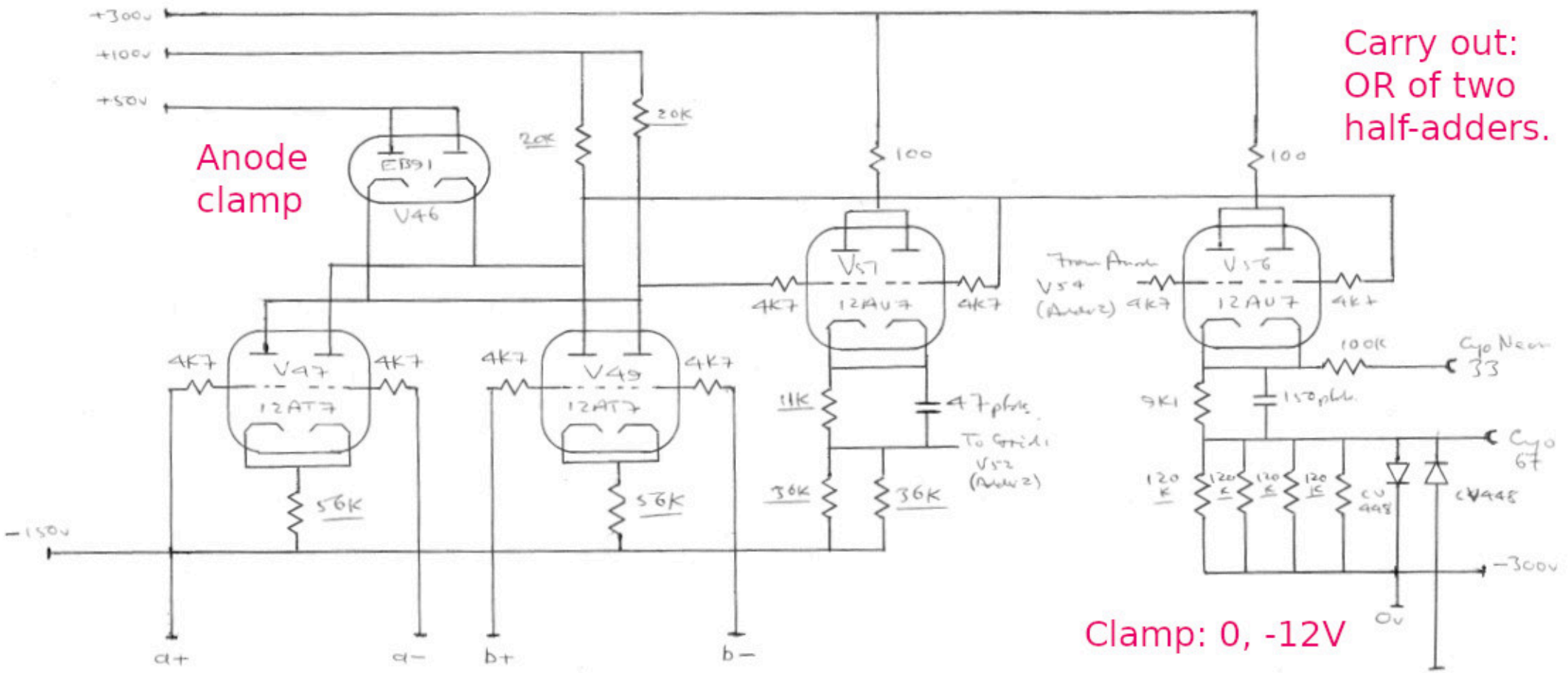
Chassis 1/2

1

Generic logic schema:



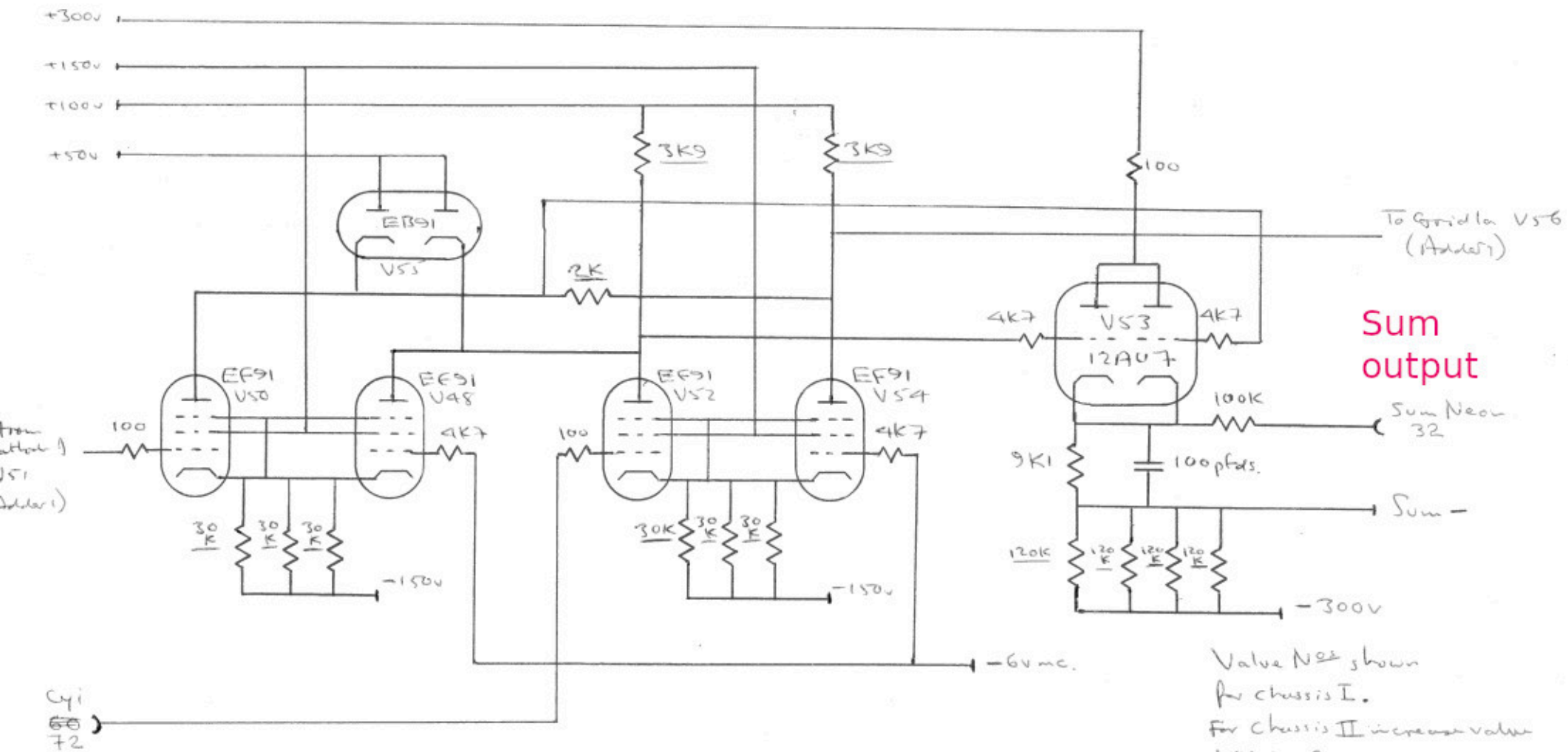
Vn	Valve N°.
P/F	Flip-Flop letter
P	Input / Output pin N°.
TU	Take-Up valve
Tr	Transfer



Value Nos shown for Chassis 1.
For Chassis 2 Value Nos
remain less 2.

The Pin connections for the
Adder on Chassis 1 & 2
are the same.

3

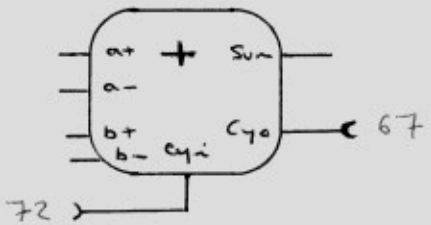


Value Nos shown for chassis I.
For chassis II increase value Nos by 2.

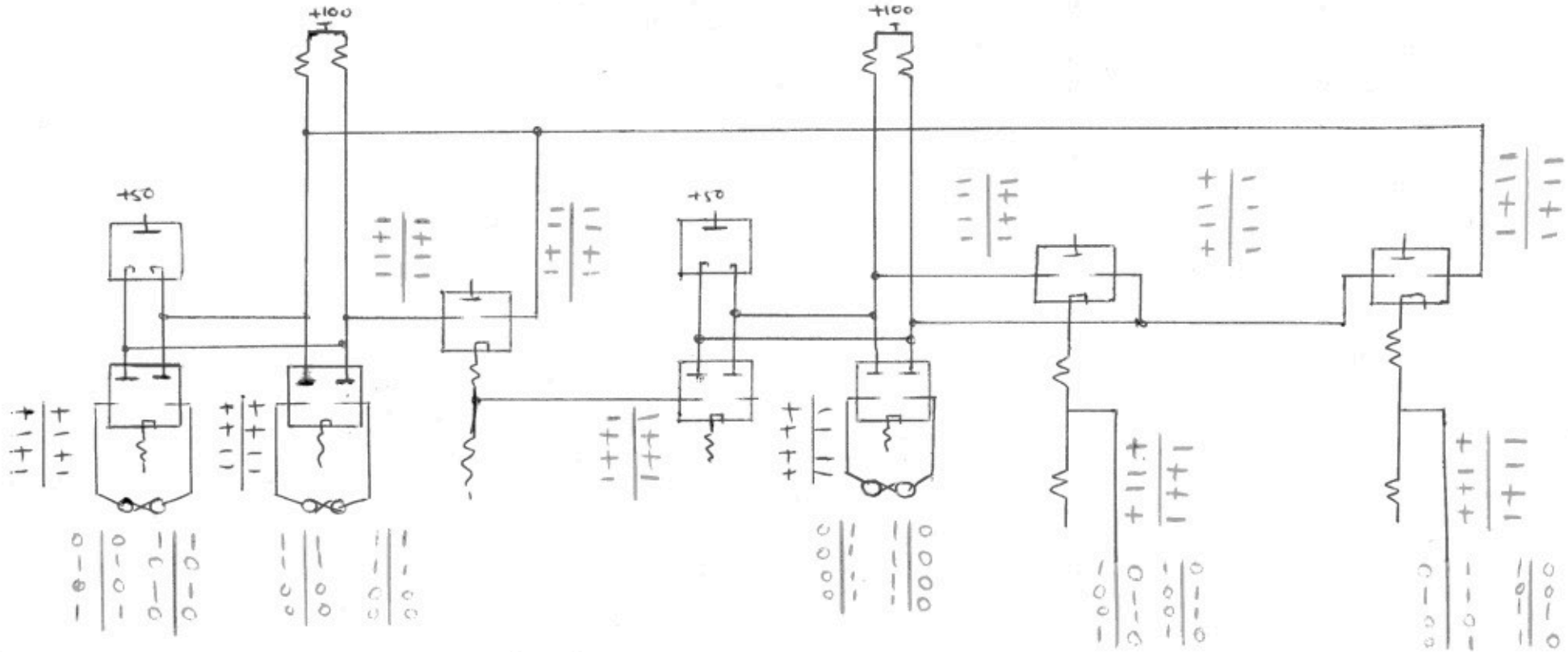
The pin connections for the Adder of chassis 1 & 2 are the same.

Chassis 1/2
Adder 2
4

Full adder schematic symbol



The Adder will be shown as above.



As Adder

M	1	1	0	0	1	1	0	0
+H	0	1	0	1	0	1	0	1
C_{yi}	0	0	0	0	1	1	1	1
Sum	1	0	0	1	0	1	1	0
C_{yo}	0	1	0	0	1	1	0	1

As Subtractor

M	1	1	0	0	1	1	0	0
−H	1	0	1	0	1	0	1	0
C_{yi}	1	1	1	1	0	0	0	0
Diff	1	0	0	1	0	1	1	0
C_{yo}	1	0	1	1	0	0	1	0

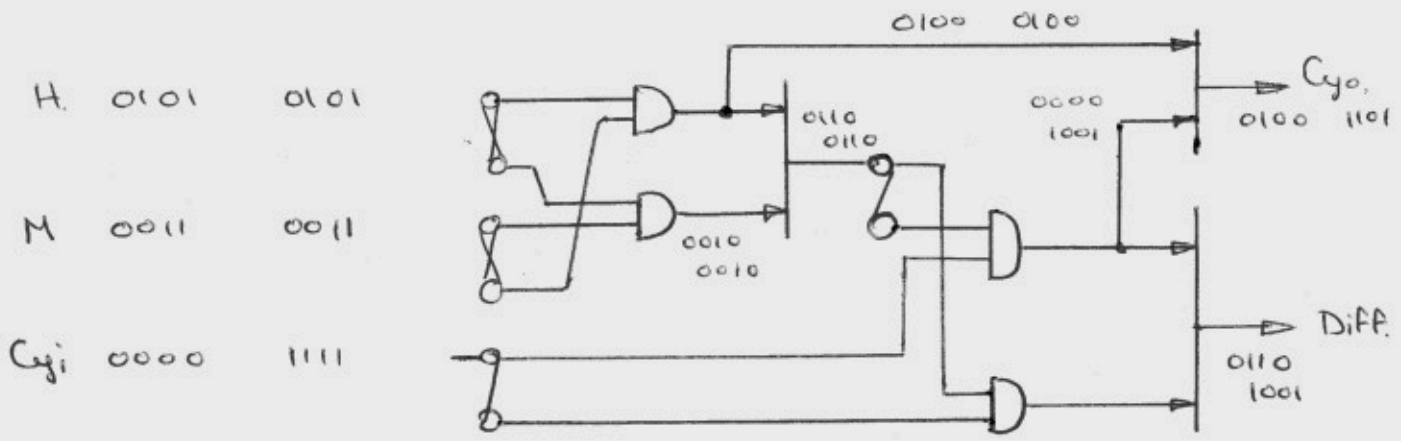
N.B That M and Sum (which is the for '1') are same for both adder & subtractor connections.

That H and C_{yi} are complemented for subtractor. (C_{yo} = same for 1's as adder).

Chassis 1/2
Adder 4

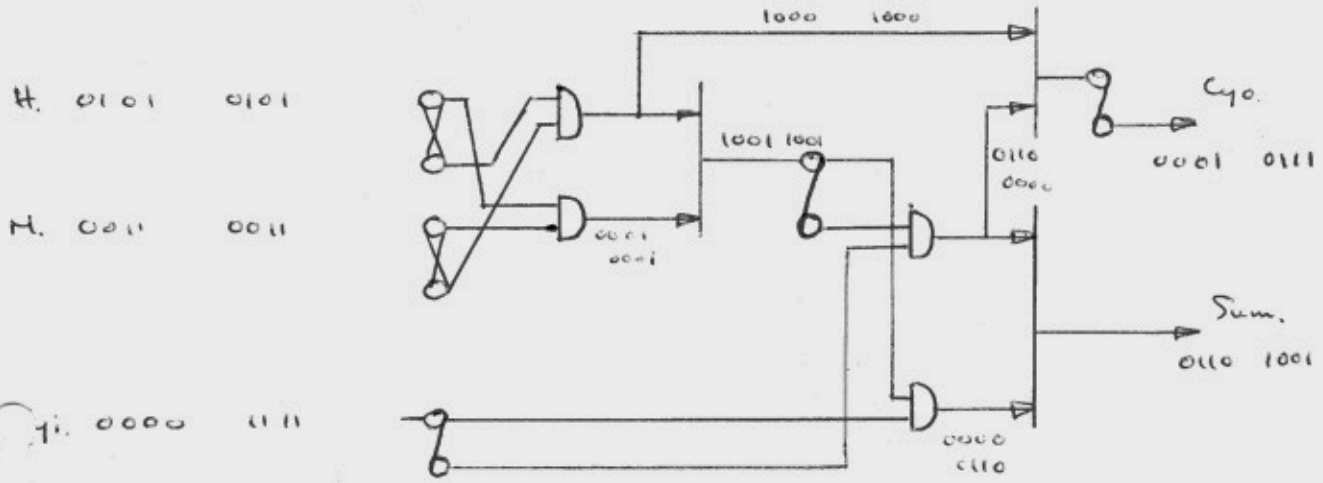
EDSAC 2 - Adders

logical



As Subtractor

M	0011	0011
H	0101	0101
Cyi	0000	1111
~H	0101	1010
Diff.	0110	1001
Cyo.	0100	1101



As Adder

M	0011	0011
H	0101	0101
Cyi	0000	1111
M+H	0110	0110
Sum	0110	1001
Cyo	0001	0111