2009 Paper 7 Question 15

Specification and Verification II

(*a*) List *two* points that compare and contrast the use of Hoare logic and Temporal logic for hardware specification and verification. [4 marks]

(*b*) What is the role of assertions in hardware verification? [4 marks]

(*c*) Explain the difference between *dynamic* and *static* assertion verification. [4 marks]

(*d*) What is the relationship between CTL, LTL and the temporal layer of PSL? What is the modelling layer of PSL? [4 marks]

(*e*) Contrast the importance of logical soundness in bug-finding and in proof of correctness. [4 marks]