COMPUTER SCIENCE TRIPOS Part II – 2026 – Paper 9

1 Advanced Computer Architecture (rdm34)

(*a*) Imagine a multicore processor where no core has a private cache. Consider the following list of configurations which describes if each core has a write buffer and if so, how it operates. In each case, what is the strongest memory consistency model (SC, TSO or relaxed) that can be supported in a straightforward manner? Briefly justify each answer.

(*i*) No write buffer. [2 marks]

(*ii*) A private non-coalescing write buffer. If a read refers to an address that has a pending write in the buffer, the buffer is flushed. [2 marks]

(*iii*) A private non-coalescing write buffer where store values from the buffer can be forwarded to loads if required. [2 marks]

(*iv*) A private coalescing write buffer where store values from the buffer can be forwarded to loads if required. [2 marks]

(*b*) Consider a simple SoC built from a general-purpose CPU, caches, and off-chip I/O. List three ways in which this design could be extended or specialised to improve performance when running a particular program. In each case, discuss both the performance benefits for the target program and the potential disadvantages for other workloads. [9 marks]

(*c*) An optimising compiler or performance-conscious programmer may apply cache blocking (also known as tiling) to improve performance. How does the presence of a multi-level cache hierarchy (e.g. L1, L2 and L3 caches) affect the application of cache blocking? [3 marks]