COMPUTER SCIENCE TRIPOS Part II – 2026 – Paper 8

1 Advanced Computer Architecture (rdm34)

(*a*) A superscalar processor may provide many more physical registers than architectural (logical) ones, in some cases ten times as many. Why is it beneficial to have so many registers? [3 marks]

(*b*) When is it safe to release physical registers so they can be reused in a superscalar processor with a unified register file? [4 marks]

(*c*) Give three reasons why VLIW architectures are commonly used in Digital Signal Processors (DSPs). [3 marks]

(*d*) You are asked to build an analytical performance model for a processor with a scalar pipeline. You are given the following parameters for a particular program and processor:

S : number of pipeline stages
B : fraction of instructions that are branches
MP : fraction of branches mispredicted
LS : fraction of instructions that are loads or stores
IM : instruction cache miss rate
IMP : instruction cache miss penalty (in cycles)
DM : data cache miss rate
DMP : data cache miss penalty (in cycles)

Assume a base (or ideal) CPI (Clocks Per Instruction) of 1.0.

(*i*) Given the parameters above, derive an expression for CPI. Given this expression, derive the total execution time T assuming a clock period P and dynamic instruction count C. Briefly describe and justify any assumptions you make. [6 marks]

(*ii*) State two reasons why your model for the pipeline's CPI could be inaccurate in practice. [4 marks]