COMPUTER SCIENCE TRIPOS Part IB – 2026 – Paper 5

8 Introduction to Computer Architecture (swm11)

(*a*) What is Moore's Law and does it still apply in 2026? [2 marks]

(*b*) Dennard scaling stopped around 20 years ago. What is Dennard scaling and what have been its effects on clock frequency scaling? [2 marks]

(*c*) How does pipelining allow clock frequency to be increased? [2 marks]

(*d*) You are asked to evaluate two scalar processor designs, Fastpath and Ecopath, that both use the RISC-V ISA RV32G. The pipelines are depicted below where: IF=Instruction Fetch, DC+RF=Decode and Register Fetch, EX=Execute (including branches), MA=Memory Access, WB=Write-back. Fastpath runs at 2GHz enabled by its pipelined instruction and data caches that take two cycles to return information but can accept a new address every clock cycle. Ecopath has single cycle caches.

Ecopath Pipeline

IF	DC+RF	EX+MA+WB

Fastpath Pipeline

IF1	IF2	DC+RF	EX	MA1	MA2	WB

(*i*) What are feed-forward paths (sometimes called *bypass paths*) and where are they needed for the two pipelines? Provide a brief rationale for each forwarding path. [4 marks]

(*ii*) Given the following memory copy code, how many pipeline stalls will each pipeline experience when executing one iteration of the loop? Assume that all memory accesses hit in the caches, that there is no branch prediction, and `a2` is initialised to 1.

```
memcpy: lw   t0, 0(a0)
        sw   t0, 0(a1)
        addi a0, a0, 4
        addi a1, a1, 4
        addi a2, a2, -1
        bge  a2, zero, memcpy
        ret
```

[4 marks]

(*iii*) When executing the `memcpy` code with `a2`=2, will Fastpath or Ecopath be fastest? Justify your answer. [4 marks]

(*iv*) What code optimisations could be applied to reduce the execution time? [2 marks]