COMPUTER SCIENCE TRIPOS Part IA – 2026 – Paper 2

2 Digital Electronics (ijw24)

(*a*) A synchronous finite state machine (FSM) using a single D-type flip-flop has its next state output given by

$$D(F, G, E, Q) = \overline{F}.\overline{G}.\overline{E}.\overline{Q} + \overline{F}.G.E + F.\overline{G}.E + F.G.(\overline{E} + Q)$$

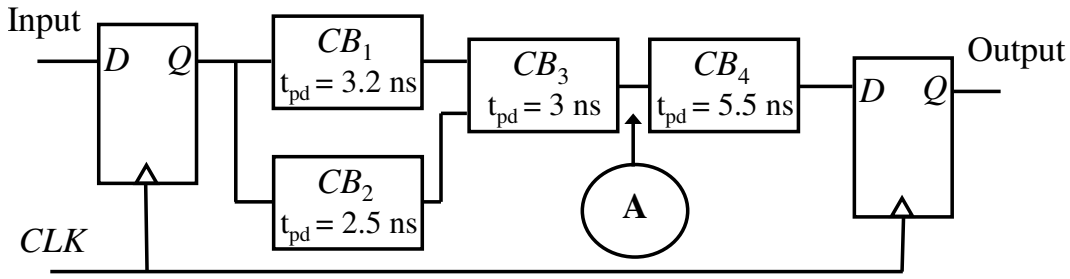
where F, G and E are inputs to the FSM, and the output of the FSM is the Q output of the flip-flop.

(*i*) Show how D could be implemented using a 4:1 multiplexer, a 2-input AND gate and a 2-input OR gate. Use F and G as the multiplexer control inputs. Assume that complemented variables are available for use. [4 marks]

(*ii*) Determine the state transition table for this FSM. [4 marks]

(*iii*) Determine the state diagram for this FSM. [5 marks]

(*b*) The following figure shows four blocks of combinational logic, CB_1 to CB_4, located between two D-type flip-flops that are clocked by the system clock, CLK. The maximum propagation delay, t_{pd}, for each combinational logic block is shown in the figure. The flip-flops have a maximum clock-to-Q propagation delay, t_{pc}= 0.2 ns, and a minimum set-up time, t_{su}= 0.1 ns.



(*i*) Determine the maximum clock frequency, i.e., the data throughput, and the time taken for one data item to pass from Input to Output, i.e., the system latency. [2 marks]

(*ii*) Now determine the data throughput and latency if an additional D-type flip-flop is inserted at position **A** in the figure. [2 marks]

(*iii*) Where might two further flip-flops be inserted to further increase throughput? What is the throughput and latency for this configuration? [3 marks]