6 Introduction to Computer Architecture (rdm34)

(*a*) You have designed a simple processor together with private instruction and data caches. You are asked to improve its performance for a particular application. You try each of the changes listed below individually but in each case the performance does not improve significantly. Describe why this might occur.

(*i*) You change the Instruction Set Architecture (ISA) and processor design to provide more registers for the compiler to use. Each instruction is now encoded using more bits. [4 marks]

(*ii*) You add a custom instruction that performs a sequence of instructions in fewer clock cycles than was previously possible. [4 marks]

(*iii*) You replace your current DRAM with a special low-latency DRAM. [3 marks]

(*iv*) You increase the associativity of the data cache from 2-way to 4-way. [3 marks]

(*b*) You add a second processor core on the same chip with its own private caches, but the speedup you achieve for a new multithreaded application is only 1.2×. What different factors could explain this limited speedup? [6 marks]