4 Operating Systems (rmm1002)

Consider a 64 bit machine architecture providing 57 bit virtual addressing using linear-address translation with a five-level page table structure in which page table entries (PTEs) are 64 bits and a page is 4096 bytes.

(*a*) Using the largest applicable SI units, how much memory can be addressed using this scheme? [2 marks]

(*b*) Show how the virtual address `0x00c0.ffee.ba5e.f00d` is translated to a physical address using the five-level page table. As well as showing how each level in the page table structure is found and indexed, you should give the size of each level in the page table in terms of both bytes and entries, and give the full size of the page table. [9 marks]

(*c*) Assume that a memory access takes 40 ns, and the machine provides a Translation Lookaside Buffer (TLB) with a hit rate of 99% and a search time of 5 ns. What is the effective memory access time? [4 marks]

(*d*) An inspired engineer suggests replacing this five-level page table structure with a simple binary trie due to its expected $\log_2(N)$ lookup performance. State whether you would expect this to perform better or worse than the five-level page table structure, and explain why. [5 marks]