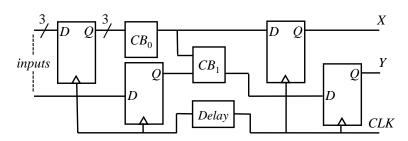
COMPUTER SCIENCE TRIPOS Part IA – 2025 – Paper 2

2 Digital Electronics (ijw24)

(a) The state transition table of a synchronous finite state machine (FSM) is

Current state	Next state				Output (Y)	
	$X_1 X_0 =$	00	01	11	10	
$\overline{S_0}$		S_0	S_1	S_1	S_1	0
S_1		S_0	S_0	S_2	S_2	1
S_2		S_0	S_0	S_3	S_0	1
S_3		S_0	S_0	S_0	S_0	1

- (i) Assuming constant inputs over multiple clock cycles, determine the repeating bit sequence at Y for each of the four input combinations $X_1X_0 = \{00, 01, 11, 10\}$. The starting state does not matter. [4 marks]
- (*ii*) Draw and label the state transition diagram for the FSM. [4 marks]
- (*iii*) The FSM is to be implemented using two D-type flip-flops FF_1 and FF_0 having outputs Q_1 and Q_0 respectively. The state assignment is: $S_0[Q_1 = 0, Q_0 = 0], S_1[Q_1 = 0, Q_0 = 1], S_2[Q_1 = 1, Q_0 = 1]$ and $S_3[Q_1 = 1, Q_0 = 0]$. Determine the simplified equations necessary to generate the output Y and the flip-flop inputs D_1 and D_0 . [5 marks]
- (b) In the following schematic diagram, the *inputs* are connected to 4 D-type flip-flops (FFs) and CLK is the system clock. The outputs from 3 of the FFs are input to combinational logic block CB_0 , and the output from the fourth FF is input to combinational logic block CB_1 . The outputs from the combinational blocks are connected to two D-type FFs with outputs X and Y. For all FFs, the set-up time $t_{su} = 50$ ps, the hold time $t_h = 60$ ps, the propagation delay (clock-to-Q) $t_{pc} = 80$ ps and the minimum propagation delay (clock-to-Q) $t_{pc} = 80$ ps. For CB_0 , the propagation delay $t_{pd,min} = 25$ ps. Unless stated otherwise, Delay has a propagation delay of $t_{skew} = 0$ ps.



(*i*) Determine the maximum clock frequency. [2 marks]

- (ii) Determine if the FF hold time constraint is satisfied. [2 marks]
- (*iii*) Now assume that $t_{skew} = 20$ ps. Determine the maximum clock speed, and whether the FF hold time constraint is now met. [3 marks]