7 Introduction to Computer Architecture (swm11)

A microprocessor design team currently has a classical five-stage pipelined processor comprising: instruction fetch, decode + register fetch, execute, data memory access, write-back. They also included independent instruction and data level-1 caches (32 KiB each) and one level-2 cache (256 KiB).

(*a*) In the context of this five-stage pipeline, explain what the following hazards are and how they might arise:

(*i*) control hazards, [2 marks]

(*ii*) structural hazards. [2 marks]

(*b*) For this five-stage pipeline, what are forwarding paths and why they are needed? Include a sketch of the pipeline indicating where the forwarding paths are located. [3 marks]

(*c*) To boost performance, new 128 KiB level-1 instruction and data caches are proposed, but these need to be pipelined to maintain the clock frequency resulting in 2-cycle access latency. The level-2 cache is boosted to 1 MiB without increasing the level of pipelining. This takes the five-stage pipeline to seven-stages.

(*i*) Sketch the new pipeline. Why might new forwarding paths be required? [3 marks]

(*ii*) What is a load-to-use penalty for the five-stage and seven-stage pipelines? [2 marks]

(*iii*) What is a branch penalty for the five-stage and seven-stage pipelines? [2 marks]

(*iv*) What is the cache access latency in cycles for each design given the following table of parameters? [4 marks]

	pipeline size	
	5-stage	7-stage
Level-1 data-cache miss rate	5%	3%
Level-2 cache miss rate	2%	1.5%
Level-1 data-cache access latency in cycles	1	2
Level-2 cache access latency in cycles	9	9
DRAM access latency in cycles	100	100

(*d*) What is tandem verification and how could the technique be used to test the

pipelined processor designs? [2 marks]