COMPUTER SCIENCE TRIPOS Part IA – 2024 – Paper 2

2 Digital Electronics (ijw24)

(*a*) A synchronous 3-bit binary counter has a mode selection input X. If $X = 1$, the counter output sequence is 0, 1, 2, 3, 4, 5, 6, 7, 0, ... (decimal), and if $X = 0$, the counter output sequence is 7, 6, 5, 4, 3, 2, 1, 0, 7 ... (decimal). The counter is implemented using three, D type flip-flops with outputs labelled $\{Q_2, Q_1, Q_0\}$, where Q_0 represents the least significant bit.

(*i*) Write down the state transition table for this counter. [2 marks]

(*ii*) Detemine in simplified sum-of-products form, the next state combinational logic required for the D type flip-flops. [6 marks]

(*iii*) Show that the next state combinational logic for the D type flip-flop with output Q_1 can also be implemented using only exclusive OR (XOR) operations and a complement operation. [2 marks]

(*b*) A Mealy finite state machine (FSM) with input X and output Z is represented by the following state transition table.

Current state (Q)	Next state (Q')		Output (Z)	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	F	0	1
E	A	F	0	1
F	G	F	0	1
G	A	F	0	1

(*i*) Use row matching to eliminate states in this FSM and give the updated state transition table. [4 marks]

(*ii*) Show if this solution yields the minimum number of states. [2 marks]

(*c*) A D type flip-flop is used as a synchroniser to reduce problems owing to metastability in a synchronous FSM. P_{fail} is the probability of an invalid logic level at the synchroniser flip-flop output for a single input change and the input to the synchroniser flip-flop changes at a mean rate of N times/s.

(*i*) For $P_{fail} = 0.01$ and $N = 0.1$, what is the mean time between failure (MTBF) of the synchroniser?

(*ii*) Determine the minimum number of similar D type flip-flops that need to be cascaded for the synchroniser to achieve a minimum MTBF of 100 days?

[4 marks]