COMPUTER SCIENCE TRIPOS Part II – 2023 – Paper 8

1 Advanced Computer Architecture (rdm34)

(*a*) The Branch Target Buffer (BTB) stores information about previously encountered branch instructions. A simple design would store the entire address of the branch instruction and an entire target address. How could the number of bits stored in each entry of the BTB be significantly reduced and what trade-offs are involved? [4 marks]

(*b*) The BTB and branch predictor are normally accessed on every clock cycle regardless of whether the instruction being fetched is a branch. Assuming a scalar processor, outline one idea that could be used to help reduce these unnecessary accesses? [4 marks]

(*c*) Modern superscalar processors are able to support hundreds of instructions "in-flight" at the same time and schedule instructions dynamically (i.e. support out-of-order execution). What advantages does dynamic scheduling offer when compared to an in-order superscalar processor? [4 marks]

(*d*) Some processors convert short-forward branches, i.e. those that branch over a few instructions, to an instruction that sets a predicate register followed by a short sequence of instructions that are conditionally executed depending on the value of the predicate.

(*i*) Why might such a scheme perform better than simply relying on branch prediction and what are its limitations? [4 marks]

(*ii*) Given a superscalar processor that supports out-of-order execution, briefly outline what changes to the processor would be required to support such a scheme. [4 marks]