6 Introduction to Computer Architecture (swm11)

Consider the following three correct state machines (seqA, seqB, seqC) written in SystemVerilog.

module seqA(input clk, input rst, output logic [3:0] a);
always_ff @(posedge clk or posedge rst)
if(rst)
a <= 0;
else
begin
a[0] <= !a[0];
a[1] <= a[0] ^ a[1];
end
endmodule

module seqB(input clk, input rst, output logic [3:0] b);
logic [3:0] n;
always_ff @(posedge clk or posedge rst)
if(rst) b <= 0;
else
begin
b[0] = (b[0] & !n[0]) ^ b[1];
b[1] = (b[1] & !n[1]) ^ b[2];
enend
endmodule

module seqC(input clk, input rst, output logic [3:0] c);
logic [15:0] s;
always_ff @(posedge clk or posedge rst)
if(rst) s <= 16’d1;
else
begin
c[2] = (|s[7:4]) | (|s[15:11]);
c[3] = |s[15:8];
end
endmodule

(a) Why is it important that an implementation of a circuit meets all timing constraints? [2 marks]

(b) What is the complete sequence that each of the three modules (seqA, seqB, seqC) outputs after reset (rst) is released? Justify your answer. [6 marks]

(c) If the three modules were mapped to an FPGA consisting of many 4-input 1-output LUTs (lookup tables), DFFs (D flip-flops) and programmable wiring, what resources would each module require for a minimal implementation? Justify your answer. [6 marks]

(d) Let us assume that LUTs have an input-to-output delay of 2d, DFFs have a setup time of d and no other delays, and we ignore wire delays. For each module, what is the minimum clock period in terms of d assuming no clock jitter? Justify your answer. [6 marks]