COMPUTER SCIENCE TRIPOS Part IB – 2023 – Paper 5

6 Introduction to Computer Architecture (swm11)

Consider the following three correct state machines (seqA, seqB, seqC) written in SystemVerilog.

```
module seqA(input clk, input rst,
                                            module seqB(input clk, input rst,
            output logic [3:0] a);
                                                         output logic [3:0] b);
                                            logic [3:0] n;
always_ff @(posedge clk or posedge rst)
                                            always_ff @(posedge clk or posedge rst)
  if(rst)
                                              if(rst) b <= 0;
    a <= 0;
                                              else
                                                      b <= n;
 else
                                            always_comb
                                              begin
    begin
      a[0] <= !a[0];
                                                n[0] = !b[0];
                       ^ a[1];
      a[1] <= a[0]
                                                n[1] = (b[0] \& !n[0]) \hat{b}[1];
                                                n[2] = (b[1] \& !n[1]) ^ b[2];
      a[2] <= &a[1:0] ^ a[2];
                                                n[3] = (b[2] \& !n[2]) \hat{b}[3];
      a[3] <= &a[2:0] ^ a[3];
    end
                                              end
endmodule
                                            endmodule
```

```
module seqC(input clk, input rst, output logic [3:0] c);
logic [15:0] s;
always_ff @(posedge clk or posedge rst)
if(rst) s <= 16'd1;
else s <= {s[14:0],s[15]};
always_comb
begin
    c[0] = s[1] | s[3] | s[5] | s[7] | s[9] | s[11] | s[13] | s[15];
    c[1] = s[2] | s[3] | s[6] | s[7] | s[10] | s[11] | s[14] | s[15];
    c[2] = (|s[7:4]) | (|s[15:12]);
    c[3] = |s[15:8];
end
endmodule
```

- (a) Why is it important that an implementation of a circuit meets all timing constraints? [2 marks]
- (b) What is the complete sequence that each of the three modules (seqA, seqB, seqC) outputs after reset (rst) is released? Justify your answer. [6 marks]
- (c) If the three modules were mapped to an FPGA consisting of many 4-input 1-output LUTs (lookup tables), DFFs (D flip-flops) and programmable wiring, what resources would each module require for a minimal implementation? Justify your answer.
 [6 marks]
- (d) Let us assume that LUTs have an input-to-output delay of 2d, DFFs have a setup time of d and no other delays, and we ignore wire delays. For each module, what is the minimum clock period in terms of d assuming no clock jitter? Justify your answer. [6 marks]