2 Digital Electronics (ijw24)

The figure below shows a circuit using an N-channel MOSFET, along with a table giving the relationship between $V_{DS}$ and $I_{DS}$ for various values of $V_{DS}$, at $V_{DD} = 4$ V and $V_{GS} = 4$ V.

![](image)

<table>
<thead>
<tr>
<th>$V_{DS}$(mV)</th>
<th>160</th>
<th>320</th>
<th>470</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DS}$(mA)</td>
<td>48</td>
<td>92</td>
<td>130</td>
</tr>
</tbody>
</table>

(a) Calculate the value of resistor $R$ and the power dissipated in it when $V_{DS} = 160$ mV. 

(b) A capacitor $C$ is connected between the source and drain terminals of the MOSFET. After the MOSFET turns OFF at $t = 0$, the output signal $V_2$ as a function of time $t$ is given by $V_2 = V_{DD}(1 - e^{-t/CR})$. Assume that prior to $t = 0$, the MOSFET is ON and $V_2 = 0$ V.

(i) Determine an expression for the time taken $t_r$, for the output signal $V_2$ to rise from 20% to 80% of its maximum value.

(ii) What is the rise time $t_r$, if $C = 0.1$ $\mu$F and $R$ takes the value calculated in Part (a)?

(iii) The value of $R$ is changed so as to reduce the rise time to half that in Part (b)(ii). What is the new value of $R$?

(iv) Using the value of $R$ calculated in Part (b)(iii), what is the power dissipated in $R$ when the MOSFET is ON (i.e., when $V_{GS} = 4$ V), and assuming that $V_2 = 320$ mV?

(v) Explain how the problem of high static power consumption seen in the N-channel MOSFET circuit can be eliminated. 

[9 marks]
(c) The logic gate in the following figure has 3 inputs, \( A, B, \) and \( C, \) and a single output \( Y. \) Determine the truth-table for the gate input to output function, and then determine a simplified Boolean expression for output \( Y \) in terms of \( A, B, \) and \( C. \)