2 Digital Electronics (ijw24)

The figure below shows a circuit using an N-channel MOSFET, along with a table giving the relationship between $V_{DS}$ and $I_{DS}$ for various values of $V_{DS}$, at $V_{DD} = 4$ V and $V_{GS} = 4$ V.

\[
\begin{array}{c|c|c|c}
V_{DS}(mV) & 160 & 320 & 470 \\
I_{DS}(mA) & 48 & 92 & 130 \\
\end{array}
\]

\(V_{1}\) \hspace{1cm} 0V

\(V_{DD}\)

\(R\)

\(V_{2}\)

(a) Calculate the value of resistor $R$ and the power dissipated in it when $V_{DS} = 160$ mV.

(b) A capacitor $C$ is connected between the source and drain terminals of the MOSFET. After the MOSFET turns OFF at $t = 0$, the output signal $V_{2}$ as a function of time $t$ is given by $V_{2} = V_{DD}(1 - e^{-t/(CR)})$. Assume that prior to $t = 0$, the MOSFET is ON and $V_{2} = 0$ V.

(i) Determine an expression for the time taken $t_{r}$, for the output signal $V_{2}$ to rise from 20% to 80% of its maximum value.

(ii) What is the rise time $t_{r}$, if $C = 0.1 \mu F$ and $R$ takes the value calculated in Part (a)?

(iii) The value of $R$ is changed so as to reduce the rise time to half that in Part (b)(ii). What is the new value of $R$?

(iv) Using the value of $R$ calculated in Part (b)(iii), what is the power dissipated in $R$ when the MOSFET is ON (i.e., when $V_{GS} = 4$ V), and assuming that $V_{2} = 320$ mV?

(v) Explain how the problem of high static power consumption seen in the N-channel MOSFET circuit can be eliminated.

[9 marks]
(c) The logic gate in the following figure has 3 inputs, \( A, B, \) and \( C, \) and a single output \( Y. \) Determine the truth-table for the gate input to output function, and then determine a simplified Boolean expression for output \( Y \) in terms of \( A, B, \) and \( C. \)