

2 Digital Electronics (ijw24)

(a) With the aid of block and example state diagrams, describe the main features of Moore and Mealy implementations of finite state machines. [6 marks]

(b) A finite state machine (FSM) takes two inputs, A and B , and generates one output, Z . The output at cycle n , Z_n , is

$$Z_n = \begin{cases} A_n \cdot A_{n-1} & \text{if } B_n = 0 \\ A_n + A_{n-1} & \text{if } B_n = 1. \end{cases}$$

(i) Determine the state transition table and the state diagram for a Mealy implementation of this FSM where the single D -type flip-flop state register has input A at its D -input. [5 marks]

(ii) Write down the Boolean functions for the next state and output combinational logic for the FSM. [2 marks]

(iii) Show how the FSM could be implemented using a 2:1 Multiplexor and some additional 2-input combinational logic gates. [2 marks]

(iv) Show how the FSM could be modified to eliminate the asynchronous changes on the output Z in response to inputs A and B . [1 mark]

(c) An FSM may be implemented using a generic logic array (GLA) device or a generic array logic (GAL) device. With the aid of diagrams, compare and contrast the architecture of GLA and GAL devices, specifically identifying the advantages and disadvantages of each device structure. [4 marks]