COMPUTER SCIENCE TRIPOS Part II – 2019 – Paper 9

4 Comparative Architectures (rdm34)

(*a*) As modern processors and system-on-chip (SoC) designs become more complex, so does the on-chip interconnect.

(*i*) Why does the design of an on-chip network differ greatly from that of larger scale networks? [3 marks]

(*ii*) Draw a diagram showing the datapath of an on-chip router with virtual channels. [3 marks]

(*iii*) How do virtual channels help to reduce packet latency? [3 marks]

(*iv*) For what reason, other than performance, may virtual-channel flow control be useful?

[2 marks]

(*b*) You have been asked to outline the design of a high-performance 16-core processor suitable for use in a server-class machine. Draw a clear block diagram illustrating your architecture. Include all the major building blocks, e.g. processor cores, caches, on-chip interconnects, memory controllers and the main off-chip interfaces. Provide a brief description of how cache coherence is maintained, what type(s) of on-chip interconnect are provided, a brief overview of the features of your individual cores and the characteristics of your caches. For each major component briefly justify your design decisions.

[9 marks]