11 Optimising Compilers (tmj32)

(a) Describe the phase-order problem in a compiler and illustrate your answer with some example code. [4 marks]

(b) You are advising a semiconductor design company on building a compiler for their latest processor. The processor has the following features:

- Sixteen 64-bit registers (r0–r15) and sixteen 32-bit registers (s0–s15), the latter corresponding to the lower 32 bits of each of the 64-bit registers.

- A one-cycle branch delay slot after each control-transfer instruction (i.e. the instruction after a branch is executed before the branch takes effect).

- Complex arithmetic instructions that implicitly use r15 as their first source operand.

What are the challenges of code generation for this processor, given these features and how can they be addressed within the compiler? [8 marks]

(c) To ease compilation, the chief designer suggests that the processor’s instructions could be executed directly in SSA form (i.e. all destination registers unique). This would use a small cache to provide fast access to the most recently used virtual registers. Discuss the advantages and disadvantages of such an approach from the compiler writer’s viewpoint. [8 marks]