(a) Describe the organisation of a two-level branch predictor that makes use of a global branch history.

(b) What are false (or name) dependencies and what hardware technique is often used to remove them within a processor?

(c) You are asked to design a new Instruction Set Architecture (ISA). You are told that this new ISA will be the basis for both simple low-power and high-performance processor implementations. Would you include the features or design choices listed below? In each case, carefully justify your answer.

(i) A branch delay slot.

(ii) The ability to predicate the execution of most instructions.

(iii) A conditional move instruction.

(iv) The use of condition codes (or flags) to specify the branch condition.

(v) A large number of general-purpose registers.

(vi) A TSO memory consistency model.

(vii) Support for custom ISA extensions, e.g. to allow the addition of special functional units.