1 Computer Design (swm11)

(a) In SystemVerilog, what is the difference between:

(i) The ternary operator ? and if...then...else statements? [2 marks]

(ii) always_ff and always_comb? [2 marks]

(iii) Blocking, non-blocking and continuous assignment? [3 marks]

(iv) Logic values 0, 1, x and z and how these values propagate through Boolean logic gates? [3 marks]

(v) The way that synchronous and asynchronous reset are declared in an always_ff statement? [2 marks]

(b) The following module attempts to implement a reset control circuit that should have the following behaviour: when the user-controlled reset button (which needs to be debounced) is pressed the asyncButton signal is high and should result in the rst going high and remaining high for a minimum of 10^6 clock cycles. rst should be generated immediately after the rising clock edge to allow time for it to propagate.

```verilog
module timeResetBad(
    input logic clk,
    input logic asyncButton,
    output logic rst);
logic ctr [18:0];
logic ctrAtMax;
always_comb begin
    ctrAtMax = &ctr;
    rst = !ctrAtMax;
end
always_ff @(posedge clk)
    ctr <= asyncButton ? 0 :
        !ctrAtMax ? ctr+1 : ctr;
endmodule
```

(i) What is wrong with the timeResetBad module? [4 marks]

(ii) Write a corrected version timeResetBad that makes minimal changes and adds no new modules. [4 marks]