1 Digital Electronics (ijw24)

(a) (i) Show that

\[ A + B.C = (A + B).(A + C) \]  

[2 marks]

(ii) Using the distributive law in Part (a)(i), express the following equation in product of sums form with 4 product terms, each with a sum of 3 variables:

\[ F = H + I \bar{J} + \bar{K}.L \]  

[4 marks]

(b) (i) Write down the truth table for the logic unit (LU) defined in the following table that can execute one of 4 logical operations at a time on 2 data inputs \((Y_1, Y_0)\), to yield output \((Z)\). The LU is under the control of inputs \((I_1, I_0)\) and the logical operations are encoded to 2-bit instruction codes as follows:

<table>
<thead>
<tr>
<th>Operation</th>
<th>Instruction code ((I_1I_0))</th>
</tr>
</thead>
<tbody>
<tr>
<td>OR</td>
<td>00</td>
</tr>
<tr>
<td>AND</td>
<td>01</td>
</tr>
<tr>
<td>XOR</td>
<td>10</td>
</tr>
<tr>
<td>NOP</td>
<td>11</td>
</tr>
</tbody>
</table>

Note that operations OR, AND and XOR have their usual meanings and that the execution of NOP implies \(Z\) can take any binary value.  

[3 marks]

(ii) Use a Karnaugh Map to determine a simplified expression for \(Z\) in Part (b)(i).  

[2 marks]

(c) (i) Show using a circuit diagram how \(W\) can be implemented in 2-level sum of products form using AND gates followed by OR gates. Remember to include any NOT gates required since only uncomplemented input variables are available:

\[ W = \overline{B}.\overline{C} + \overline{A}.B.C + A.C.\overline{D} \]  

[2 marks]

(ii) Consider the implementation in Part (c)(i). Assume that the gates have finite propagation delay. Describe what happens at \(W\) when inputs \(\{A, B, C, D\}\) change from \(\{1, 0, 1, 0\}\) to \(\{1, 0, 0, 0\}\).  

[3 marks]

(iii) Determine the other single input variable change that will give a similar problem to that observed in Part (c)(ii).  

[2 marks]
(iv) Determine a modified sum of products expression for $W$ that will eliminate the problems observed in Part (c)(ii) and Part (c)(iii).

[2 marks]