

2 Comparative Architectures (RDM)

- (a) Total Store Order (TSO) is a widely implemented memory consistency model. How does TSO differ from Sequential Consistency (SC)? [4 marks]
- (b) Describe an execution of a simple program that is legal under TSO but not SC. The simple program should consist of two threads, each thread consisting of a small number of load and store instructions accessing memory locations X and Y. [3 marks]
- (c) Would the use of a coalescing write buffer violate TSO? Justify your answer. [4 marks]
- (d) Consider a chip-multiprocessor where each core supports simultaneous multi-threading (SMT). Furthermore, each processor core has a write-through L1 data cache. Could multicopy atomicity be supported in such a design? [6 marks]
- (e) Consider a chip-multiprocessor with two cores P1 and P2. Coherence is maintained using a MESI protocol with support for Bus Upgrade (**BusUpgr**) transactions to avoid unnecessary data transfers (i.e. when moving from state S to M). Why might a processor that initially makes a **BusUpgr** request have to change the request to a Read-Exclusive (**BusRdX**) before it even wins access to the shared bus? [3 marks]