3 Computer Design (TMJ)

(*a*) A processor's main memory is usually implemented using DRAM.

(*i*) Describe a typical DRAM cell. [2 marks]

(*ii*) Show, with the aid of a diagram, how DRAM is organised, making reference to devices, ranks, banks and arrays. [4 marks]

(*iii*) Describe the difference between an open-page and closed-page row-buffer policy and the types of access patterns they benefit. [2 marks]

(*b*) The MOSI cache coherence protocol adds a new owned (O) state to the basic MSI protocol.When a cache holding a line in M state snoops a read request from another cache, it transitions to O state and forwards the data to the requestor. Subsequent snoops for read requests are also fulfilled by this owner cache. An owned line is dirty and only one cache can hold a line in O state at any time.

(*i*) Describe the difference between cache coherence and memory consistency. [2 marks]

(*ii*) Draw a state transition diagram for the MOSI protocol, using a new action *Forward* to indicate data being forwarded from one cache to another. [6 marks]

(*iii*) Draw a table showing how the state of a line in one cache limits the states the same line can have in a different cache. [2 marks]

(*iv*) Give two benefits of adding this extra owned state to the basic MSI protocol. [2 marks]