1 Computer Design (SWM)

(a) Given an active high reset signal, how is an asynchronous reset described in SystemVerilog? [2 marks]

(b) For each of the following six `always_ff` blocks, what sequence or error will be produced and why? You should assume `clk` is a clock and that all registers are reset to zero at the start (as they are for FPGAs). [3 marks each]

```verilog
logic [2:0] rb, rc, rd, re, rf, rg;
always @(negedge clk)
$display("rb=%d rc=%d rd=%d re=%d rf=%d rg=%d",
rb, rc, rd, re, rf, rg);

always_ff @(posedge clk)
rb <= (rb<6) ? rb+1 : 0;

always_ff @(posedge clk)
begin
  if(rc>=6) rc <= 0;
  rc <= rc+1;
end

always_ff @(posedge clk)
begin
  rd <= rd+1;
  if(rd>=6) rd <= 0;
end

always_ff @(posedge clk)
begin
  if(re>=6) re = 0;
  re = re+1;
end

always_ff @(posedge clk)
if(rf<6) rf <= rf-14;
else rf <= 0;

always_ff @(posedge clk)
casex(rg)
  3'b0??: rg<=rg+1;
  3'b11?: rg<=0;
endcase
```