COMPUTER SCIENCE TRIPOS Part II – 2018 – Paper 7

5 Comparative Architectures (RDM)

(*a*) Briefly describe three microarchitectural techniques or elements that can be used to improve the performance of a scalar pipelined processor. You are unable to fetch more than a single instruction per clock cycle or make any changes to the Instruction Set Architecture (ISA). [4 marks]

(*b*) Imagine two processor implementations with equal performance. One is a superscalar design with support for out-of-order execution. The other is an in-order scalar processor. In what circumstances might the superscalar design be more power efficient? [6 marks]

(*c*) Loads and stores are often reordered in a superscalar processor. Describe how some loads can be issued speculatively before the addresses of older stores are known and how mispredictions are detected and handled. [6 marks]

(*d*) How can memory reference speculation be supported in a VLIW processor? [4 marks]