1 Computer Design (SWM)

(a) Write one or more lines of SystemVerilog that correspond to a complete module for each of the following circuits. Aim for simplicity and explain any subtleties of your implementation.

(i) Write a complete SystemVerilog module for the circuit shown.

(ii) Write a complete SystemVerilog module for the circuit shown.

(iii) Write a complete SystemVerilog module for the circuit shown.
(b) Consider the following SystemVerilog module:

```verilog
module gcd(
    input logic clk,
    input logic rst,
    input logic start,
    input logic [15:0] Ain,
    input logic [15:0] Bin,
    output logic [15:0] answer,
    output logic done
);

logic [15:0] a, b;
always_ff @(posedge clk or posedge rst)
    if(rst)
        begin
            a <= 0;
            b <= 0;
            answer <= 0;
            done <= 0;
        end
    else
        if(start)
            begin
                a <= Ain;
                b <= Bin;
                done <= 1'b0;
            end
        else if(b==0)
            begin
                answer <= a;
                done <= 1'b1;
            end
        else if(a>b)
            a <= a-b;
        else
            b <= b-a;
endmodule
```

(ii) What values of Ain and Bin will cause the module to fail to terminate (i.e. done will never go high)? [2 marks]