2 Digital Electronics (IJW)

(a) Give the truth table for an RS Latch implemented using two cross coupled NOR gates and determine the state diagram for the $\overline{Q}$ output. [6 marks]

(b) Give the truth table for a 2-to-4 decoder (i.e., 2 control inputs, $S_1, S_0$, and 4 outputs, $Q_3, Q_2, Q_1, Q_0$) and show how it can be implemented using 2-input NOR and NOT gates. [4 marks]

(c) Show how the 2-to-4 decoder in part (b) can be used to implement a 4-to-1 multiplexor (i.e., 4 inputs, 2 control inputs and 1 output) using only NAND gates for the additional combinational logic required. [4 marks]

(d) (i) Write down the state transition table corresponding to the following state diagram

where $[Q_B Q_A]$ are the current state, $B$ and $A$ are the inputs, and $X$ and $Y$ are the outputs.

(ii) Show how two D-type flip flops and two 4-to-1 multiplexors can be used to implement the Mealy machine given in the state diagram in part (d)(i). [6 marks]