COMPUTER SCIENCE TRIPOS Part IB – 2016 – Paper 5

2 Computer Design (SWM)

(*a*) Why is there a risk of data and control hazards in a pipelined processor? [4 marks]

(*b*) For modern RISC instruction set architectures like RISC-V, why are control hazards not exposed in the programming model? [4 marks]

(*c*) How might data hazards be mitigated in each of the three pipelines below? [6 marks]

Pipeline A:

instruction fetch	decode	register fetch execute memory access write-back

Pipeline B:

instruction fetch	decode register fetch	execute memory access write-back

Pipeline C:

instruction fetch	decode register fetch	execute	memory access	write-back

(*d*) Do exceptions introduce a control hazard? Give justification for your answer. [3 marks]

(*e*) Do interrupts introduce a control hazard? Give justification for your answer. [3 marks]