

COMPUTER SCIENCE TRIPOS Part IB – 2015 – Paper 5

3 Computer Design (TMJ)

(a) Consider a multicore processor running the MSI cache coherence protocol in each core's private caches. The caches are connected to each other and memory via a snoopy bus.

(i) What is a cache coherence protocol and in what systems is it needed? [4 marks]

(ii) What events would lead a cache to issue a bus transaction if it holds a block of data in state S? [4 marks]

(iii) When and why does data need to be flushed back to memory in this protocol? [4 marks]

(b) (i) What are the semantics of load linked and store conditional instructions? [4 marks]

(ii) Describe the synchronisation method that the following code performs by adding comments to it.

```
membar
label1: ll    r2, 0(r1)
        sub  r2, r2, #1
        sc   r2, 0(r1)
        beqz r2, label1
label2: load r2, 0(r1)
        bneq r2, label2
```

[4 marks]