1 Computer Design (SWM)

Below is a SystemVerilog module (`shaft_decoder`) and its test bench (`run_test`).

```
module shaft_decoder(
    input              clock,
    input              reset,
    input [1:0]        grey_code,
    output logic [7:0] position);

   logic   previous_code;
   always_ff @(posedge clock)
    case({previous_code, grey_code})
      4'b00_01, 4'b01_11, 4'b11_10, 4'b10_00: position <= position+1;
      4'b00_10, 4'b10_11, 4'b11_01, 4'b01_00: position <= position-1;
    endcase
endmodule


module run_test();
   logic clock;
   logic reset;
   logic [1:0] grey_code;
   logic [7:0] position;

   shaft_decoder dut(.clock, .reset, .grey_code, .position);

   initial begin
       clock = 1;
       reset = 1;
       grey_code = 2'b00;
   #10 reset = 0;
   #10 grey_code = 2'b01;
   #10 grey_code = 2'b11;
   #10 grey_code = 2'b10;
   #10 grey_code = 2'b00;
   #10 grey_code = 2'b10;
   #10 grey_code = 2'b11;
   #10 grey_code = 2'b01;
   #10 grey_code = 2'b00;
   #10 grey_code = 2'b10;
   #10 grey_code = 2'b01;
   #30 $finish;
   end

   always #5 clock = !clock;

   always @(posedge clock)
     $display("%05t: grey_code=%2b position=%03d",
              $time,grey_code,position);

endmodule
```

The `shaft_decoder` module takes a two-bit grey-code sequence from an optical shaft encoder (e.g. one of the two directions on a mechanical mouse) and outputs an 8-bit position. When the shaft is rotating in the positive direction, the following sequence of inputs is seen: 00 → 01 → 11 → 10 → 00. The shaft is rotating in the negative direction if the reverse sequence is seen. When the shaft is not moving, the input does not change. Inputs arrive asynchronously.

(*a*) The `shaft_decoder` module is syntactically correct but functionally slightly erroneous. What are the errors? [8 marks]

(*b*) In the `run_test` module:

(*i*) At what times will clock edges be produced (in simulation time units) and when will reset be deasserted? [4 marks]

(*ii*) What will be the output sequence for `position` for the whole simulation? [4 marks]

(*c*) What are the advantages of simulation over test on reconfiguration hardware? [4 marks]