2011 Paper 2 Question 2

Digital Electronics

(a) Show how two 2-input NOR gates can be connected together to implement an RS latch. Describe its operation and give its truth table. [6 marks]

(b) Draw the state diagram for a synchronous modulo-4 up/down counter. The counter has two control inputs: M is set at logic "0" to cause the counter to count up, and at logic "1" to cause the counter to count down; E is set at logic "1" to enable the counter to count and at logic "0" to cause the counter to hold its current state. [4 marks]

(c) A synchronous binary up-counter having the state sequence

$$1, 2, 3, 4, 5, 6, 1, 2, \ldots$$

is to be implemented using three D-type flip-flops. The flip-flop outputs are designated Q_2, Q_1 and Q_0, where Q_0 represents the least significant digit of the count.

   (i) Give simplified expressions for the required next-state logic, making use of any unused states. Does this counter self-start? [6 marks]

   (ii) Give the new simplified expression required for D_0 (the D-input of flip-flop Q_0) if the counter is now required to return to a count of 1 if an unused state is entered. [4 marks]