2009 Paper 9 Question 13

Specification and Verification II

(*a*) What is the "false-implies-everything" problem? [2 marks]

(*b*) What is the difference between temporal and data abstraction? [2 marks]

(*c*) How do models of combinational and sequential devices differ? [2 marks]

(*d*) How is the rising edge of a signal modelled in higher order logic? [2 marks]

(*e*) Write down a formula that asserts that if a signal s has the value `a` then at all later times it also has the value `a`. [2 marks]

(*f*) Give *two* properties of transistors that are not modelled by the simple switch model. [2 marks]

(*g*) What are advantages of using binary decision diagrams to represent Boolean formulae? [2 marks]

(*h*) What is the difference between linear and branching time? [2 marks]

(*i*) What are the relative expressive powers of LTL and CTL? [2 marks]

(*j*) How do the Verilog and VHDL simulation cycles differ? [2 marks]