Comparative Architectures

(a) How does the use of condition codes (also known as condition bits or status flags) complicate the implementation of a superscalar processor that supports out-of-order execution? [4 marks]

(b) A branch predictor with a high prediction accuracy is often employed to enable deeply pipelined processors to be exploited. What limits the complexity and size of such a branch predictor? [4 marks]

(c) In the best case, how can a branch predictor and branch target buffer enable a branch instruction and the instruction at the branch’s target address to be fetched in consecutive clock cycles? [6 marks]

(d) Loop unrolling and predicated execution are two techniques that may be used to improve the performance of loops.

(i) How do these techniques improve performance? [3 marks]

(ii) What costs or disadvantages are associated with each technique? [3 marks]