2008 Paper 9 Question 2

VLSI Design

(a) A full adder for a single bit has three inputs, a, b and c_{in}, and two outputs, s and c_{out} for the sum and carry-out. State the formulae for s and c_{out} in disjunctive normal form. [2 marks]

(b) Explain the operation of the following three approaches for handling carry in n-bit word adders, deriving formulae for the signals involved and explaining the limiting factors on their speed:

(i) ripple carry, [2 marks]

(ii) carry-skip with fixed-size blocks, and [6 marks]

(iii) carry-skip with variable-size blocks. [4 marks]

(c) Assuming a delay of τ for a round of combinational logic consisting of negation, conjunction and disjunction, estimate the delays for the three designs applied to a 48-bit adder. [3×2 marks]