

2008 Paper 8 Question 2

VLSI Design

- (a) Sketch a transistor-level circuit for the function $\overline{A \cdot B + C \cdot D}$ in static CMOS. [4 marks]
- (b) Annotate the circuit to indicate the widths of the transistors required to give rise and fall times equal to a minimal, balanced inverter. Assume that p-channel transistors have γ times the resistance of n-channel transistors when conducting. [4 marks]
- (c) Calculate the logical effort and parasitic delay for the circuit. [4 marks]
- (d) Sketch a stick diagram for the circuit, arranged for reasonably compact layout. Assume two layers of metal with power and ground routed in parallel tracks on the second layer, and arrange for inputs and the output to be available outside the power rails. [4 marks]
- (e) Estimate the size of your layout, assuming a separation of 8λ between the centre-lines of parallel metal tracks. [4 marks]