2008 Paper 12 Question 2

Computer Design

(*a*) The classic MIPS 5-stage pipeline is depicted below.

instruction fetch	decode and register fetch	execute	memory access	write back

    (*i*) With reference to the 5-stage pipeline, what are *data hazards* and how can they be resolved to ensure that the programmer's model of sequential execution is always preserved whilst minimising performance impact?

                                                   [6 marks]

    (*ii*) With reference to the 5-stage pipeline, what are *control hazards* and how can they be resolved? [4 marks]

(*b*) If we wanted the above pipeline to mimic two processors running at half the speed, then we could have two copies (A and B) of the register state and keep the existing pipeline. The instruction–fetch stage would alternate between fetching from threads A and B on alternate clock cycles. As a consequence, if instruction fetch was from thread B, then an instruction from thread A would be in decode, B in execute, A in memory access and B in write back.

    (*i*) For this dual-threaded processor, if branches are performed in the decode stage, does the pipeline exhibit a branch delay slot? [5 marks]

    (*ii*) How can the resolution of data hazards be simplified for this dual-threaded processor? [5 marks]