## 2008 Paper 11 Question 2

## **Digital Electronics**

- (a) With the aid of relevant diagrams, show the effect on the output of a combinational logic circuit of a:
  - (i) static hazard;
  - (ii) dynamic hazard.

[3 marks]

- (b) Simplify the following expressions using Boolean algebra:
  - (i)  $X = (A + \overline{B} + \overline{A} \cdot B) \cdot (A + \overline{B}) \cdot \overline{A} \cdot B$

(ii) 
$$Y = (A + \overline{B} + \overline{A} \cdot B) \cdot \overline{C}$$
 [4 marks]

(c) Given:

$$F = A \cdot B \cdot \overline{C} \cdot D + A \cdot C + B \cdot \overline{C} \cdot \overline{D} + \overline{B} \cdot C + \overline{A} \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot D$$

Show using a Karnaugh map that F can be simplified to

$$F_1 = A \cdot B + \overline{A} \cdot \overline{B} + A \cdot C + B \cdot \overline{C} \cdot \overline{D}$$
 [2 marks]

- (ii) Show that there are a total of four possible expressions for F. [3 marks]
- (iii) Show how  $F_1$  can be implemented using NAND gates and draw the circuit diagram. Assume that complemented input variables are available.

[2 marks]

- (iv) Show how the static 1 hazard in  $F_1$  can be eliminated using a Karnaughmap-based approach. [2 marks]
- (v) Now implement  $F_1$  assuming that only 2-input NAND gates are available. [4 marks]